Constant Current Forming in Amorphous Silicon Semiconductor Memory Devices

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A thesis submitted for the degree of Doctor of Philosophy.

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To my parents and my family.

Abstract

This thesis describes the forming process under *constant current* conditions of Cr/p^+a-Si:H/V thin film devices (a-Si:H denotes hydrogenated amorphous silicon). In the initial stages of electro-forming by constant current stressing, with increasing injection of charge via either increasing bias or time, the $J-V$ characteristics of devices exhibit an instability, as shown by a decrease in the reverse current. This is interpreted in terms of the creation of defects in the a-Si:H. The defect generation rate, as measured by the voltage shift ΔV at a constant reverse current in the $J-V$ curves, is found to follow a square-root time-dependent law. Eventually, with further increasing current bias, the local current density reaches a critical value J_F, and a rapid 'runaway' process occurs, which results in an irreversible change of the initial high-resistance state into a permanent 'formed' state of lower resistance.

It has also been observed that formed samples sometimes show a metal-non metal (MNM) transition at low temperatures ($60-100K$). The electrical properties of these devices have been analysed in detail. The ac characteristic can be modelled using multi-component RC and RL equivalent circuits below and above the MNM transition region. An anomalous frequency dependence of the capacitance is explained in terms of a percolation-like critical behaviour of the dielectric constant ϵ_{eff}, which enhances notably at the percolation threshold p_c. A general approach for activated tunnelling in granular thin films is used to explain electron transport in formed devices. Analysis shows that the structure of formed Cr/p^+a-Si:H/V devices structure can be modelled as a heterogeneous filamentary medium composed of metallic particles and an insulator host (e.g.a-Si:H). The metallic particles originate from the diffusion of the top vanadium electrode during the forming process. This model is consistent with memory characteristics, such as the change in activation energy with device resistance.

Declaration of originality

This thesis was composed entirely by myself. The work reported herein was conducted exclusively by myself in the Department of Electronic and Electrical Engineering at the University of Edinburgh.

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Contents

List of Figures

List of Tables

List of principal symbols

A^*	effective Richardson constant
$B_3{}^0$	inactive threefold-coordinated boron
$B_4{}^0$	neutral boron substitution site
$B_4{}^-$	ionised acceptor states
C_g	gas phase impurity concentration
C_m	capacitance of a metallic particle
D_H	hydrogen diffusion coefficient
D^0	or $Si_4{}^0$, neutral dangling bond
D^+	or $Si_3{}^+$, positive charged defect states
D^-	or $Si_3{}^-$, negative charged defect states
dV/dI	Dynamic resistance
E_A	energy at the edge of the conduction band tail
E_B	energy at the edge of the valence band tail
E_C	conduction band (or mobility) edge
E_F	Fermi level
E_G	mobility gap ($= E_C - E_V$)
E_V	valence band (or mobility) edge
E_a	thermal activation energy of conduction (for unformed samples)
E_b *or* ϕ	Schottky barrier height
$E_b(x)$	barrier profile

E_{ch}	charging energy of a metallic particle
$G(0,T)$	zero-bias dynamic conductance
h *or* $\hbar$	Planck constant ($\hbar \equiv h/2\pi$)
I_{bias}	stress bias during current stressing
J_0 *or* I_0	current density (current) prefactor
J_s	reverse saturation current
k_B	Boltzmann constant
L	device thickness
m_0	electron mass
m^*	effective mass
N_D	dangling bond density
N_a	acceptor density
N_d	donor density
$P_3{}^0$	inactive threefold-coordinated phosphorus
$P_4{}^0$	neutral phosphorus substitution site
$P_4{}^+$	ionised donor states
p	volume fractions of metallic particles
p_c	percolation threshold
Q_f	injected charge in current stressing
q *or* e	electronic charge
q	critical exponent (in §5.2 and §9.3.4)
R_m	room temperature analogue memory resistance
T_e	electron temperature in plasma
T_{eff}	effective electron temperature in bulk a-Si:H
T_{tr}	transition temperature in metal-non metal transition samples
T_m	characteristic temperature of unstressed samples
T_s	substrate temperature during the deposition of a-Si:H
V_R	reverse voltage

V_{mea}	change in voltage across the sample during current stressing
V_0	magnitude of V_{mea}
x	ac conductance exponent
y	ac dielectric constant exponent
α	effective tunnelling constant [defined as $(k_BT/q)\partial J/\partial \mathcal{E}$]
α_T	temperature coefficient of resistance (TCR)
β	dispersion parameter
ΔE	thermal activation energy of conduction (for formed samples)
ΔV	voltage shift during current stressing
ΔV	switching voltage width (in §4.1.2 and §4.1.3)
Δn_{BT}	excess carrier density in the band tail
$\mathcal{E}$	electric field
ϵ	dielectric constant ($= \epsilon_0\epsilon_s$)
ϵ_{eff}	effective dielectric constant
ϵ_h	dielectric constant of a host material
ϵ_s	relative dielectric constant of the semiconductor ($\epsilon_s = 11.7$ for a-Si:H)
η_g	gas doping efficiency
μ	electron drift mobility
ϕ_I	barrier height with contribution of the image force
ϕ_{eff}	effective barrier height
$\overline{\phi}$	average barrier height
ρ^+	net positive space charge density
ρ^-	net negative space charge density
σ_{ext}	conductivity in the extended states
σ_{hop}	hopping conductivity
σ_{min}	the minimum metallic conductivity
σ_{tail}	hopping conductivity in the band tail
τ	relaxation time constant

Chapter 1

Introduction.

This study concerns the electrical properties of hydrogenated amorphous silicon (a-Si:H) thin film memory switching devices having metal/p^+a-Si:H/metal structures, with an emphasis on those characteristics associated with current forming and related phenomena.

Owen *et al* [21] in 1982 first reported memory switching in $p^+ - n - i$ structures of a-Si:H prepared by the glow discharge technique. Compared with electronic switching in chalcogenide materials these devices exhibited extremely fast transition times, non-volatile, and polarity dependent memory switching properties. Later a-Si:H memory devices with a simpler metal/p^+/metal structure were also developed which could be formed with much lower voltages and with analogue as well as digital switching characteristics [10]. Extensive studies of the a-Si:H memory device have been carried out over a wide range of its properties, including device structure [10,21,22], the forming process [11,12], dynamic characteristics during device operation [7,10,21,23], the memory mechanism [10,24], quantised electron effects [25–27], and applications in analogue neural networks [28,29], *etc.*

In all a-Si:H memories, of whatever structure, an electro-forming process is required before they function as switching devices. Electro-forming greatly reduces the device resistance (typically from $10^6 - 10^{10}\Omega$ to $10^2 - 10^5\Omega$) and causes a modification of the original structure of the a-Si:H network (forming is discussed in more detail below and in §4.2). As a result, the electronic state

can be reversed to the OFF state by a suitable current (energy) pulse. It has been established by various experiments that a highly conducting filament is built up in the a-Si:H during the forming process [22,24]. Attempts have also been made to attribute the observed memory operation (i.e. from ON-state to OFF-state, or vice versa) and other related phenomena (i.e. the quantisation effect), to the existence of the filament [10, 24]. However, there exists no satisfactory theory which can explain all the important characteristics of a-Si:H memory devices. The main reason for this is the extremely fine microstructure of the filament, which makes it difficult to probe and model. Voltage-pulse biasing has generally been the method of forming the metal/p^+a-Si:H/metal devices. It is known to cause an irreversible change which, when localised in a small area, creates a permanent filament, which is estimated to be $\leq 0.5\mu$ in diameter [11]. Some of the top metal contact is also incorporated into the changed microstructure of the filament, either by diffusion or by electro-migration, or a combination of both.

Forming the metal/p^+a-Si:H/metal devices under constant current conditions, as an alternative to voltage-pulsing, was first investigated by Scott [18]. He showed that it was indeed possible to form the devices using a small current over a long period of time. Another interesting finding by Scott was that some formed devices exhibit a metal-non metal (MNM) transition at low temperature. Specifically, the dc resistance of the devices undergoes a continuous change at about $60K$, from semiconductor-like behaviour to metallic, as the temperature increases. It was not understood at the time whether the MNM transition was related to the conducting filament or was simply a contact effect. More work is needed to clarify the physical mechanisms responsible for both the current forming process and the MNM transition.

This study is an extension of the preliminary work done by Scott on current forming, and it is devoted mainly to two topics: 1) the electrical properties of devices under constant current stress and forming; 2) an analysis of the metal-non metal transition in formed devices.

In the following chapters, brief introductions to the material properties of a-Si:H and metal/a-Si:H Schottky barriers are given in *Chapter* 2 and *Chapter* 3 respectively. A more detailed description of the characteristics of a-Si:H memory devices and the voltage-bias forming is given in *Chapter* 4. The main properties of granular metal films, such as activated tunnelling and metal-non metal transitions, are described briefly in *Chapter* 5. Experimental details are given in *Chapter* 6, followed by results on the basic properties of unstressed (origin) devices in *Chapter* 7. *Chapter* 8 describes and discusses the experimental results on constant current stressing and forming. The MNM transition and its relevance to switching mechanism are considered, in details, in *Chapter* 9. *Chapter* 10 is a final summary of the work and the conclusions, with some suggestions for further research.

Chapter 2

Material Properties of a-Si:H.

2.1 Preparation and structure of a-Si:H.

2.1.1 Preparation.

Hydrogenated amorphous silicon (a-Si:H) was first made by Chittick *et al* in the late 1960s by the glow discharge (GD) plasma decomposition of silane gas, SiH_4 [30]. Although other deposition methods, such as sputtering, photo-CVD, *etc*, can be also used, GD deposition is still the most commonly used technique, as it generally gives better quality a-Si:H films. Further description of the depositions of a-Si:H will be given later in *Chapter* 6 when discussing the experimental details. During deposition, silane SiH_4 is admitted into the chamber and is decomposed in the plasma area between the substrate and the powered electrode.

Hydrogen is involved in the chemical reaction on the growing surface. It can react at the a-Si:H surface and produce dangling bonds either by releasing itself from Si-H bonds or by breaking Si-Si bonds. Hydrogen can also bond itself to unsaturated Si so as to eliminate dangling bonds [31]. It is now generally believed that during the growth of a-Si:H there is a chemical equilibrium between the strained (or weak) silicon bonds (Si-Si) and dangling bonds (D^0), with the mediation of hydrogen, [32, 33]. The equilibrium reactions exist not only on the growing surface, but also in the bulk of a-Si:H during and after deposition. The main electronic and structural properties of a-Si:H, such as the density of

states, doping, and many metastable changes, can be understood on the basis of the equilibration theory.

2.1.2 Silicon bonding structure in a-Si:H.

The structure of a-Si:H is characterised mainly by short range order and long range disorder, and is usually described using a continuous random network (CRN) model [34]. According to the CRN model, each atom in a random network, no matter whether it is host or impurity, has its normal number of bonds to its immediate neighbours (the coordination). This is in marked contrast to a crystalline lattice in which impurities are generally constrained to have the coordination of the host because of the long range ordering of the lattice. Fig. 2.1 illustrates a two-dimensional a-Si:H network containing atoms of different coordination (4, 3, and 1). This feature of the a-Si:H structure has an important effect on doping and electrical properties and is discussed in §2.3. The four-fold silicon bonding structure is overcoordinated according to

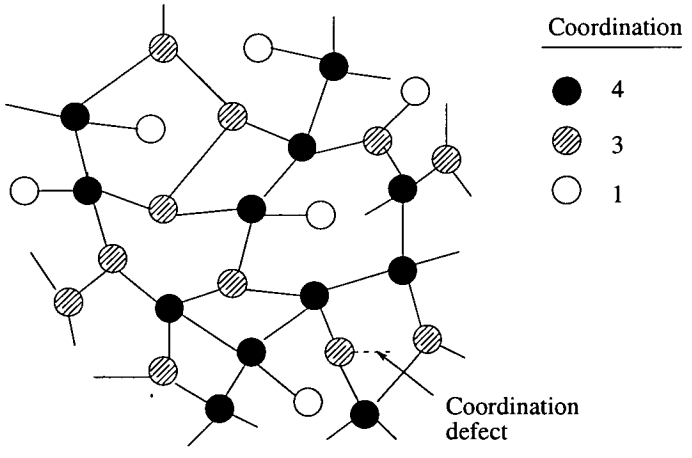


Figure 2.1: A schematic representation of a continuous random network containing atoms of different bonding coordinations.

Phillips' analysis of the relation between network coordination and disorder [35]. He found that for a three-dimensional continuous random network, the ideal coordinating number per atom should be 2.45 if each atom still keeps three degrees of freedom. In a-Si:H, the existence of hydrogen helps to reduce

the network coordination because it forms only a single bond to silicon and does not link the network together. However the hydrogen content is only $\sim$ 10% in the best quality a-Si:H films, which is far less than that required ($\geq$ 50 %) to achieve the overall network coordination of 2.45, thus a-Si:H remains a rigid structure and is mechanically hard [35,36].

2.1.3 Hydrogen bonding structure in a-Si:H.

Hydrogen in a-Si:H mainly bonds with Si atoms, effectively reducing the defect density in the film. Hydrogen atoms have three main bonding configurations with Si atoms: SiH, SiH_2, and SiH_3. In each configuration, there are two or more vibrational modes because a single hydrogen atom has three degrees of freedom.

In contrast with silicon atoms which bond in a structure of a rigid overcoordinated network with a high strain energy, hydrogen is more weakly bound and can diffuse within the material at moderate temperatures of around two hundred degrees centigrade. Experiments have revealed that hydrogen diffusion in a-Si:H is thermally activated and also strongly doping-dependent [1,2]. Fig. 2.2 shows the change of hydrogen diffusion coefficient D_H with temperature in a wide doping range of donors (P) and acceptor (B). The greatest change is with p-type material for which D_H is increased by a factor 10^3 at $250°C$, while the increase is less in n-type material and no change is found in compensated a-Si:H. Thermally activated diffusion of hydrogen is explained by a trapping mechanism. The sources of traps are the dangling bond sites, i.e. broken $Si-H$ bonds. Hydrogen diffusion occurs by breaking a $Si-H$ bond and reforming the bond at a new site. Thus hydrogen motion can lead to either defect creation or elimination. It is hydrogen motion that causes metastable changes in the electronic properties of a-Si:H, as described in more detail in §2.4.

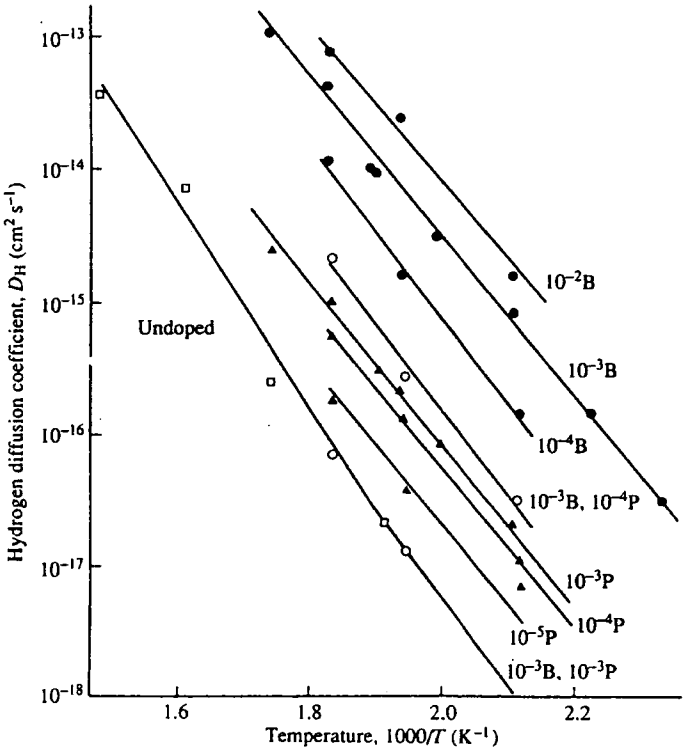


Figure 2.2: Temperature dependence of the hydrogen diffusion coefficient in a-Si:H, at different doping levels. The gas doping ratio is expressed as [Concentration of Impurity]/[SiH_4] (from Carlson *et al* [1] and Street *et al* [2]).

2.2 Electronic structure and transport mechanisms.

The electronic structure of a-Si:H comprises the bands, the band tails and defect states in the gap. Compared with its crystalline counterpart, a-Si:H has similar shapes for both conduction and valence bands due to the preservation of short range order. However, its long range structural disorder leads to the most significant difference from the crystal at the band edges where the disorder creates a tail of localised states extending into the forbidden gap. In addition, electronic states appear deep within the gap as a result of the various defects in the film, such as coordination defects. Fig. 2.3 is a schematic diagram of the band structure of a-Si:H. The states within the bands are called extended states and they are separated from band-tail states by mobility edges E_C and E_V, respectively. The mobility gap is usually taken to be $(E_C - E_V)$ $(1.6 - 1.8\,eV)$, the energy difference between extended states in the valence

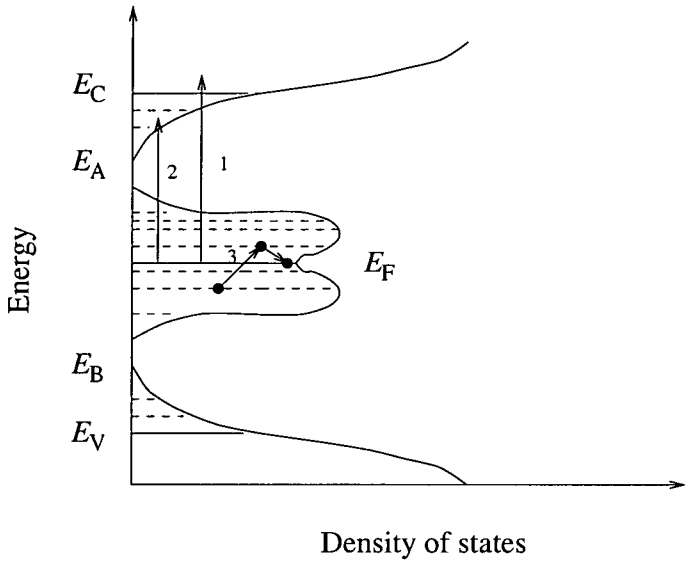


Figure 2.3: Schematic diagram of the band structure of undoped a-Si:H. Different transport mechanisms are indicated as numbers (see text for details).

band and extended states in the conducting band. The band tail states lie between E_C and E_A or E_B and E_V. The distribution is approximately exponential for low defect density a-Si:H. There is usually a slightly longer tail of valence band states above E_V than that of conduction band states below E_C. In optimally grown undoped a-Si:H the neutral-defect concentration $[D^0]$ deep in the gap is typically $10^{16}cm^{-3}$ or less [37]. According to the theory of defect formation [38], these defects are in chemical equilibrium with the weak silicon bonds in the valence-band-tail (of the order of $10^{19}cm^{-3}$).

The three main electronic (or hole) transport mechanisms in a-Si:H result directly from the electronic structure. In extended conduction band states, for example, above E_C, electron conduction is mainly by thermal activation of carriers from E_F to above the mobility edge (process 1) and follows the relation

$$\sigma_{ext} = \sigma_{min} exp(-\frac{E_C - E_F}{k_B T}) \tag{2.1}$$

where E_C is the energy corresponding to the conduction band mobility edge (see Fig.2.3), and σ_{min} is the conductivity when $E_F = E_C$, that is the min-

imum conductivity of σ_{ext} ($100 \sim 600\,\Omega^{-1}cm^{-1}$). Mott referred to σ_{min} as "the minimum metallic conductivity" [39]. The carrier mobility μ_{ext} at room temperature is estimated to be in the range of $5 - 10\ cm^2V^{-1}s^{-1}$. The activation energy $(E_C - E_F)$ is the separation of the conduction band mobility edge from the Fermi energy, and varies from nearly 1 eV in intrinsic a-Si:H to 0.1 eV in n-type material.

According to Anderson's localisation theory, carriers in localised states (either tails or gap states) cannot conduct at zero temperature [40]. At elevated temperature, however, conduction by hopping from site to site is possible. At very low temperature, conduction is dominated by variable range hopping (process 3), which obeys an equation of the form [41]:

$$\sigma_{hop} = \sigma_1 exp(-\frac{A}{T^{\frac{1}{4}}}) \tag{2.2}$$

In the band tail, hopping conduction (process 2) is given by,

$$\sigma_{tail} = \sigma_2 exp(-\frac{E_A - E_F + \Delta W}{k_B T}) \tag{2.3}$$

where E_A is the energy at the edge of the conduction band tail (see Fig 2.3) and ΔW is the average activation energy between two localised states, of the order of $10^{-2}\ eV$.

Similar relationships apply to hole conduction.

2.3 Doped a-Si:H.

Doping in a-Si:H is significantly different from that in crystalline silicon. The neutral substitution site ${P_4}^0$ (or ${B_4}^0$) is unstable in a-Si:H due to the overco-ordination mentioned in § 2.1.2. Most P and B atoms incorporated in a-Si:H act as electrically inactive threefold-coordinated structures (${P_3}^0$ and ${B_3}^0$), since they are the most stable configurations in an unstrained network. However, a few ionised donor states ${P_4}^+$ (or acceptors ${B_4}^-$) can co-exist with charged

defect states D^- (or D^+), with a rather higher total energy than ${P_3}^0$ (or ${B_3}^0$) [32,42]. The fraction of these fourfold-coordinated dopants is determined by the following thermodynamic equilibrium equations during growth:

$$ {P_3}^0 + D^0 \longleftrightarrow {P_4}^+ + D^- \; or \; {B_3}^0 + D^0 \longleftrightarrow {B_4}^- + D^+ \tag{2.4} $$

The gas doping efficiency, η_g is quite low in a-Si:H. Typically, $[P_4]/[P_3] \leq 10^{-2}$ [43]. In spite of the very low doping efficiency, the conductivity can be enhanced by several orders of magnitude compared with undoped a-Si:H and is accompanied by a large shift in the Fermi level [19].

On the other hand, doping of a-Si:H leads predominately to an increase in the charged-defect density [44–46]. Experimentally, the defect density increases with the square root of the gas phase impurity concentration, C_g [36]:

$$ N_D = 3 \times 10^{19} {C_g}^{\frac{1}{2}} \;\; (cm^{-3}) \tag{2.5} $$

Fig. 2.4 shows the distribution of charged defects in doped a-Si:H, inferred from experimental data [46]. It is seen that the defects are located at a position

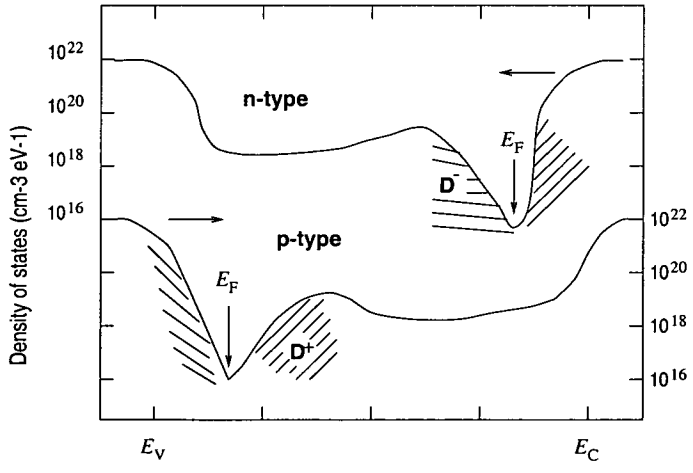


Figure 2.4: The density of states in doped a-Si:H. The shaded regions indicate states introduced by doping (from Street [3]).

close to E_F in the gap. The equilibrium between threefold-coordinated and fourfold-coordinated dopants, expressed by Eq.(2.4), can be changed by an

external stimulus. By increasing the temperature [2, 33, 47] or by applying a reverse-bias [48], some $P_3{}^0$ (or $B_3{}^0$) impurities are transformed into the electrically-active $P_4{}^+$ (or $B_4{}^-$). Decreasing temperature causes the opposite effect of dopant passivation. The activation and passivation of the donors (or acceptors) was found to be time-dependent. In almost all cases of dopant passivation, the relaxation of band-tail carriers follows a stretched-exponential time dependent law [47–49]:

$$\Delta n_{BT}(t) = \Delta n_{BT}(0) exp[-(\frac{t}{\tau})^{\beta}] \tag{2.6}$$

where Δn_{BT} is the excess carrier density, τ is the relaxation time constant which is thermally activated with an activation energy of 1 eV [36, 50, 51], and β is the dispersion parameter which is also temperature dependent [36, 52]. During the creation of active dopants, a similar time-dependent relation between Δn_{BT} and relaxation time was also found [47]. However, under a reverse-bias, Liu and Spear reported an exponential time-dependent increase in Δn_{BT} instead of that expressed by Eq.(2.6). [48].

2.4 Metastability in a-Si:H.

In 1977 Staebler and Wronski found that the dark conductivity and photoconductivity of glow-discharge-deposited a-Si:H can be reduced significantly by prolonged illumination with intense light [53]. The changes were found to be reversible by annealing at elevated temperature ($\geq 150°C$). Staebler and Wronski attributed the observed metastable changes to a reversible increase of the density of gap states acting as recombination centres for photo-excited carriers and leading to a shift of the dark Fermi level E_F toward midgap.

Stutzmann *et al* carried out a systematic study of the Staebler-Wronski effect (SWE in short) in intrinsic a-Si:H, using electron-spin resonance (ESR) and photoconductivity (PC) as the experimental tools to monitor reversible changes [54]. They reported that the SWE in pure and undoped a-Si:H is a

bulk effect caused by the creation of dangling-bond-like defect states, resulting from the breaking of bonds intrinsic to an amorphous network. The rate of creation of new dangling bonds decreases with the square of the density of already existing dangling bonds:

$$\frac{dN_D}{dt_{ill}} \propto \frac{1}{{N_D}^2} \tag{2.7}$$

where N_D is the dangling bond density, and t_{ill} the illumination time. For sufficiently long illumination times, N_D has a sublinear relation with both the illumination intensity and illumination time ($N_D \propto G^{2/3} t_{ill}^{1/3}$). This indicates that the SWE is self-limiting. The physical reason for this is that the tail-to-tail transitions leading to the creation of metastable dangling bonds are effectively shunted by recombination events via the main recombination centres, the existing stable or metastable dangling bonds. Stutzmann *et al* further suggested that dangling bonds are created as a result of weak Si-Si bond breaking instead of Si-H bond breaking, as the latter requires a higher energy (e.g. $\geq 3.5eV$).

After the work of Staebler and Wronski, it was further discovered that metastable changes of conductivity in a-Si:H can also be initiated by other means including current, electric field, doping, and rapid thermal quenching *etc*, and that these effects exist not only in intrinsic a-Si:H, but also in doped materials and alloys, and in diodes. The recombination of electron-hole pairs provides a mechanism similar to the above light-induced defect creation, with the kinetics described by a sublinear time dependence, $t^{1/3}$. However, in some cases, the stretched-exponential time dependence shown in Eq.(2.6) has also been observed [47, 55, 56]. Jackson explained this phenomena by assuming that the rate of defect formation is proportional to both the density of band-tail carriers and the rate at which hydrogen diffuses towards defect formation sites [56]. According to this model, the micro-mechanism of the metstable change is closely associated with the motion of hydrogen. When light, or a field or current is applied to a-Si:H, excess carriers are produced in the band tail, which may disrupt weak Si-Si bonds by occupying antibonding states [2]. The defect is

stable only if a hydrogen atom diffuses to the site creating metastable dangling bonds. The dangling bond left by the hydrogen atom traps the band-tail carriers and thus reduces the carrier density. Consequently, further dangling-bond creation decreases.

Chapter 3

Metal/a-Si:H Schottky Barriers.

3.1 Metal/a-Si:H Schottky barrier.

As introduced in *Chapter* 2, long range structural disorder in a-Si:H leads to a tail of localised states at the band edges and deep inside the forbidden gap. This feature of the band structure affects the distribution of space charge in a metal/a-Si:H barrier. Spear *et al* have discussed the properties of a-Si:H Schottky barriers in detail, and shown that the space charge densities are no longer a constant (equal to the donor or acceptor densities), as in a metal-crystalline barrier, but instead they change with both position and energy, due to the existence of the localised states in the energy gap [4]. Fig. 3.1 shows the net positive and negative carrier densities in a barrier region where the barrier height is E_b. The calculation is based on the density-of-state distribution measured from field-effect experiments. When $E_b = 0$ the figure refers to the bulk properties, where the acceptor density ${N_A}^- = (p^+ - n^-)$ (or ${N_D}^+ = (n^- - p^+)$ for n-type samples). Within the barrier region, an increase in E_b (or the bending of the bands) causes a change of occupancy of some of the states. The net positive space charge density is given by

$$\rho^+(E_b) = \mid e \mid {N_D}^+ - \mid e \mid (n^- - p^+) \qquad (n - type) \tag{3.1}$$

or

$$\rho^-(E_b) = \mid e \mid {N_A}^- - \mid e \mid (p^+ - n^-) \qquad (p - type) \tag{3.2}$$

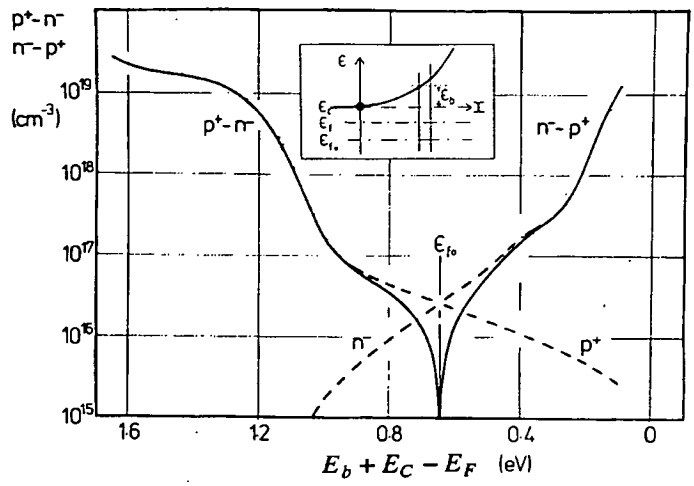


Figure 3.1: Charge densities $(p^+ - n^-)$ and $(n^- - p^+)$ as a function of the Fermi level position $(E_C - E_F)$ at room temperature (from Spear *et al* [4]).

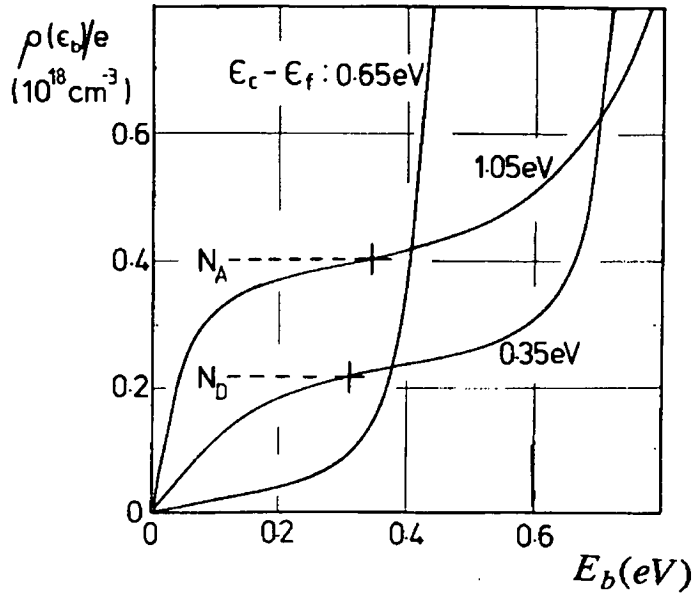


Figure 3.2: Net space charge densities ρ^+/e and ρ^-/e as a function of the barrier height E_b with different Fermi level position $(E_C - E_F)$. The dashed lines indicate the ionised acceptor densities (from Spear *et al* [4]).

It is apparent that the number of states that change their occupancy depends on the position of Fermi energy or the doping level. For a fixed Fermi level, once E_b exceeds $(E_F - E_{F0})$, the charge in the gap states will change sign; for example, it becomes negative from $\mid e \mid (p^+ - n^-)$ to $\mid e \mid (n^- - p^+)$ in the case

of p-type specimens, which makes $\rho^-(E_b)$ even larger than $\mid e \mid N_A{}^-$, as shown in Fig. 3.2.

The barrier profiles for a range of doping levels for an n-type a-Si:H Schottky barrier is shown in Fig. 3.3. For undoped or lightly doped samples the profile

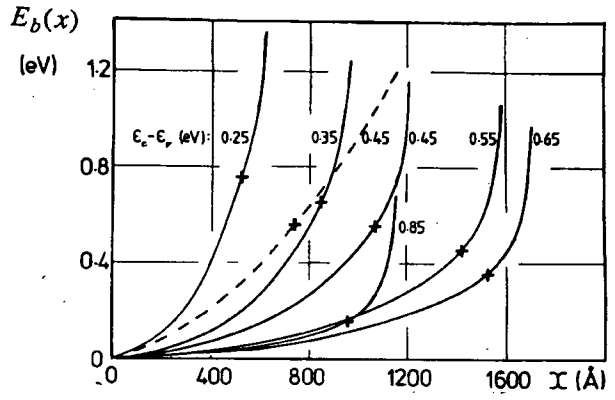


Figure 3.3: Barrier profile $E_b(x)$ of an n-type a-Si:H barrier for different positions of the Fermi level ($E_C - E_F = 0.25 - 0.85eV$). The dashed curve indicates the result with a constant space charge density at $E_C - E_F = 0.45eV$ (from Spear *et al* [4]).

changes slowly with $E_b(x)$ when $E_b(x) < 0.4eV$, but increases more sharply at larger $E_b(x)$. This is due to the effect from the charge distribution of the localised states as shown in Fig.3.2. A similar barrier profile characteristic can be found in p-type samples. If the barrier height is known the depletion width at any given doping concentration can be read off directly from these curves. On applying a forward (or reverse) voltage V to the a-Si:H barrier, the barrier height reduces (or increases) from E_b to $E_b \pm \mid e \mid V$, provided that the applied voltage is small enough not to disturb the Fermi level in the depletion region [57, 58]. In this case, the change in the barrier height occurs simply along the barrier profile shown in Fig.3.3.

3.2 Thermionic-field emission transport mechanisms.

In the case of low fields, light-doping, and intermediate temperature ranges, the dominant current transport mechanism within a Schottky barrier is either

diffusion/drift in the barrier region [59,60] or thermionic emission of electrons from the semiconductor over the top of the barrier into the metal [61–63]. Field emission (or quantum mechanical tunnelling) will prevail if (1) the temperature is low enough to eliminate transport over the barrier; (2) the doping of the semiconductor is sufficient large so as to narrow the depletion width and increase the field in the barrier, and/or (3) the reverse bias is large enough. Fig. 3.4 illustrates the band diagram for a metal/n-a-Si:H Schottky barrier

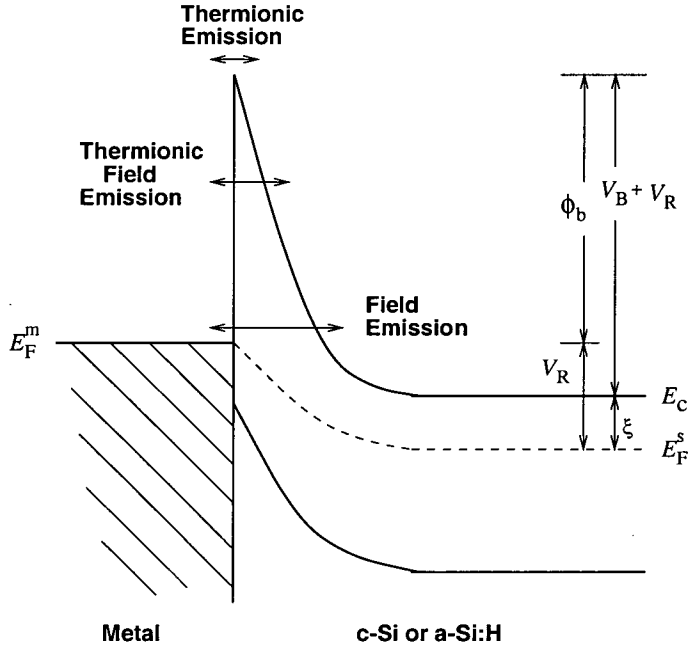


Figure 3.4: Band diagram for a metal/n-a-Si:H Schottky barrier. Different current paths for various transport regimes are also indicated.

with different current paths. In case (3), according to Padovani *et al*, the reverse biased current-voltage characteristic with tunnelling contributions at moderate values of voltage is given by [64,65].

$$J = J_s exp(V_R/E') \tag{3.3}$$

where J_s is the reverse saturation current, V_R is the reverse bias voltage, and E' is given by

$$E' = \frac{E_{00}}{qE_{00}/k_BT - tanh(qE_{00}/k_BT} \tag{3.4}$$

The term E_{00} (in V) is independent of temperature and given by

$$E_{00} = \frac{\hbar}{2}\sqrt{\frac{N}{m^*\epsilon_s}} = 18.5 \times 10^{-12}\sqrt{\frac{N}{m^*\epsilon_s}} \tag{3.5}$$

where N is the carrier concentration, m^* is the effective mass in terms of m_0, the free-electron mass, and ϵ_s is the relative dielectric constant of the semiconductor. The parameter E_{00} is, physically, the barrier height where the tunnelling probability is e^{-1} for an electron at the semiconductor band edge. Thus the parameter (qE_{00}/k_BT) gives a rough measure of the relative importance of tunnelling. When $(qE_{00}/k_BT) << 1$, thermionic emission is dominant, while field emission prevails if $(qE_{00}/k_BT) >> 1$. For $(qE_{00}/k_BT) \sim 1$, both thermionic and field emission contribute to the current. The effective barrier height ϕ_{eff} in this case is given by

$$\phi_{eff} = \frac{k_BT}{q}(\frac{\phi}{E_0} - \frac{V_R}{E'}) \tag{3.6}$$

where $E_0 = E_{00}coth(qE_{00}/k_BT)$. Eq.(3.6) predicates the barrier height ϕ_{eff} decreases linearly with increasing reverse bias.

In the high field region, i.e. when the field at the interface exceeds $2\times10^5 V/cm$, according to Shannon, the thermionic-field emission current through a barrier can also be expressed phenomenologically as [66,67]

$$J = A^*T^2exp[-\frac{q(\phi - \alpha \mid \mathcal{E} \mid)}{k_BT}] \tag{3.7}$$

where $\mathcal{E}$ is the electric field and α is an effective tunnelling constant, defined as $(k_BT/q)\partial J/\partial\mathcal{E}$.

The thermal activation energy E_a and current prefactor J_0, which reflects the current transport, are also found to change strongly with reverse bias, particularly at high field. Fig. 3.5 shows calculated results for a metal/Si/metal barrier, based on the above model [5]. It shows that the activation energy at

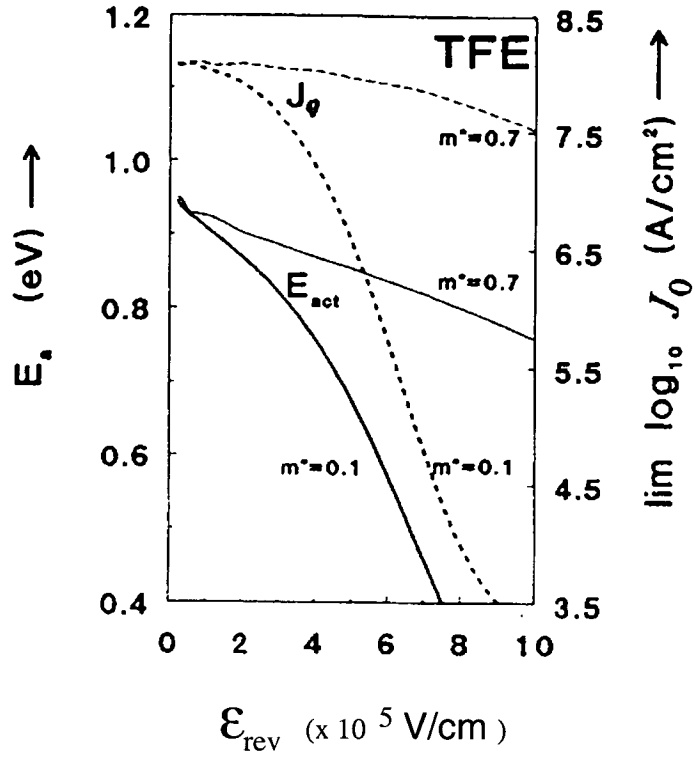


Figure 3.5: Bias dependence of E_a and J_0 in the case of thermionic-field emission (from Nieuwesteeg *et al* [5]).

low bias is close to the (temperature-independent) barrier height of $\sim 0.9eV$. The decrease at low fields is due to the image-lowering of the barrier height, evidenced by the slow change in J_0. However, the rapid reduction in E_a at high fields should result from tunnelling through the depletion potential, which effectively lowers the mean potential energy at which carriers move through the interface. Note that J_0 also decreases rapidly at high fields. The effective mass m^* also affects the behaviour of both E_a and J_0 at high fields.

The above models, when applied to doped crystalline semiconductors, have yielded results which are in fair agreement with experiments. In the case of metal-a-Si:H diodes, these models might underestimate the effects of tunnelling, due to the exclusion of the effect of the band tails on the electron distribution. Moreover, the role of hydrogen in the formation of the barrier has not been considered. Nevertheless, it has been shown that the agreement between theory and experiment is remarkably close in either doped or intrinsic a-Si:H diodes. Snell *et al* carried out a model calculation of metal/a-

Si:H barriers which included consideration of the distribution of gap states. Their results show that the current-voltage characteristics of doped Au/a-Si:H barriers can be well explained using the theory of thermionic-field emission mentioned above, when the doping level increases to $N_d \sim 10^{18} cm^{-3}$ [6].

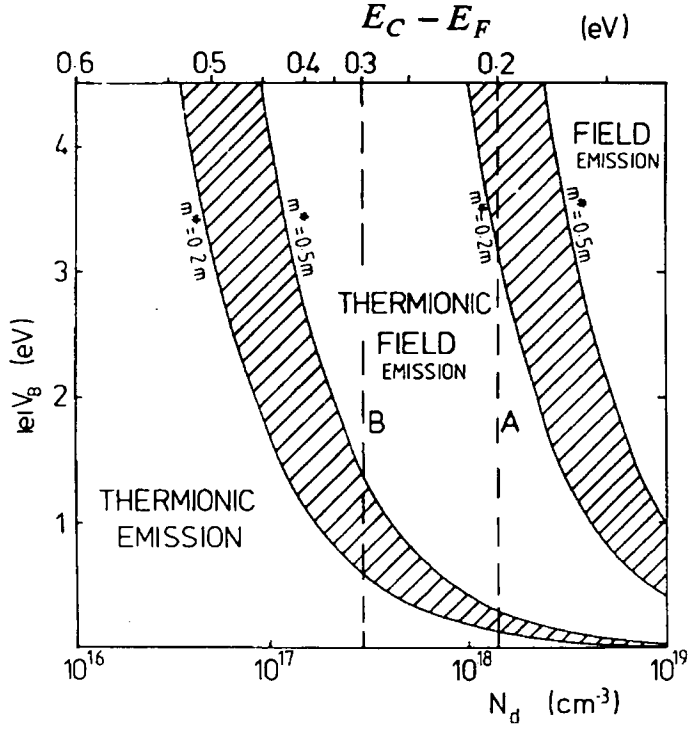


Figure 3.6: Various conduction mechanisms in a-Si:H/metal barriers as a function of band bending V_B and doping density, at $300K$ (from Snell *et al* [6]).

Fig. 3.6 illustrates different transport regimes in relation to the band bending $\mid e \mid V_B$ and the doping density at $T = 300K$. It is seen from the figure that heavy doping will shift the current transport in a-Si:H barriers from thermionic field emission to field emission, in agreement with the experimental results. The rapidly increasing breakdown current is likely to be associated with field emission. Similar results were also obtained in phosphorus-doped Pt/a-Si:H barriers by Jackson *et al* [68]. They measured changes in the effective barrier height ϕ_{eff}, determined from the spectral dependence of the photoconductivity, with both the reverse bias and doping concentration. When the doping level is over 10 *ppm*, ϕ_{eff} begins to exhibit a strong dependence on doping, and

reduces significantly even at zero field due to the high defect density. The dominant current path is no longer over the top of the barrier but moves to lower energy (roughly half the height of the barrier).

Chapter 4

a-Si:H Switching Devices and the Forming Process.

This chapter describes the main characteristics of a-Si:H switching devices, the voltage-biased forming process, and theoretical modelling of the forming and memory mechanism. Current stressing in a-Si:H will be also reviewed.

4.1 Characteristics of a-Si:H switching devices.

4.1.1 General switching phenomenon.

In general, electronic switching phenomena in amorphous semiconductors or insulators can be divided into two main categories: threshold and memory switching. Figs. 4.1(a) and (b) show the current-voltage characteristics of these two different types of switching. In the case of threshold switching (Fig.4.1(a)), once the applied bias reaches V_{TH} (the threshold voltage) the voltage across the device drops rapidly along the load line until it reduces to V_H (the holding voltage). The device is now in the ON-state, and will be maintained in the ON-state as long as the the current does not drop below I_H (the holding current) which is maintained by the electric field. When the external electric field is removed the device current reduces and the device reverts to its low-conducting OFF-state. Therefore, threshold switching is non-permanent. Memory switching exhibits a different switching scheme (as shown in Fig.4.1(b)), where both

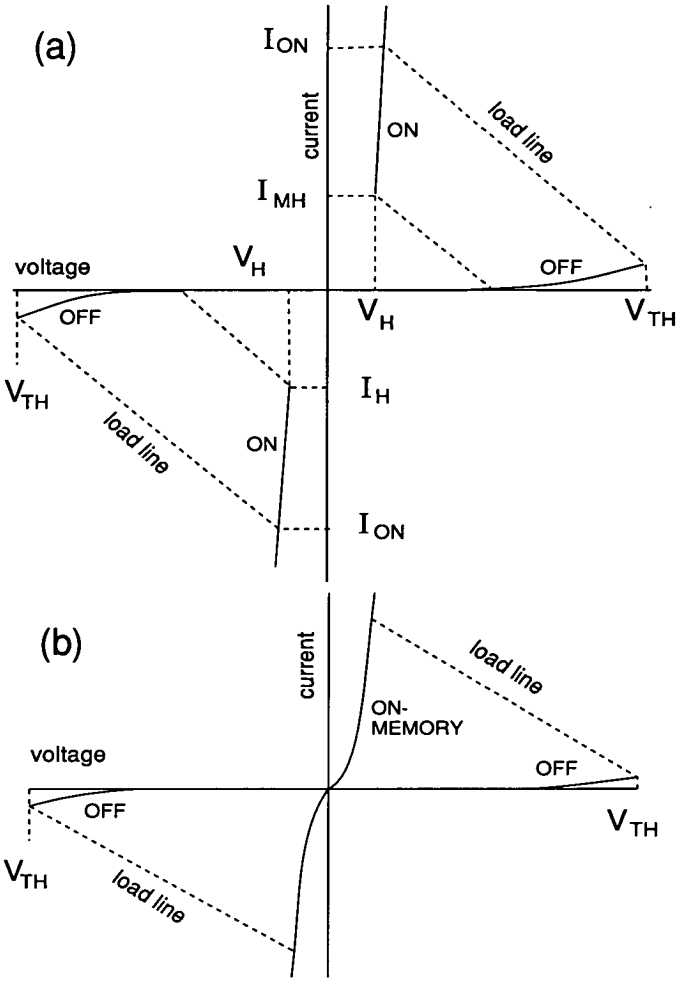


Figure 4.1: Schematic representation of switching. (a) threshold switching, and (b) memory switching.

ON- and OFF-state characteristics extrapolate through the current-voltage origin. After the first switching event from a low-conducting OFF-state to the ON-state, a permanent filament of highly-conducting material is created between the two electrodes. The device can remain in its ON-state even if the external electric field is removed. The subsequent switching between the ON and OFF-states is realised by applying suitable voltage pulses (i.e $1-5V$, $10-100ns$ in a-Si:H memory devices). This kind of device is permanent, or non-volatile, so it is termed a memory device. If there is a continuous range of intermediate states between the OFF-state and ON-state, memory switching can be further divided into two different categories, digital and analogue switching.

An initial process called *forming* is necessary for newly prepared devices to exhibit either threshold or memory switching effects. The forming voltage biasing the sample is always higher in magnitude than subsequent switching pulses. As a result, this process usually leads to irreversible change in the electrical properties of the device, i.e. a substantial reduction in the resistance. In amorphous thin-film structures, the permanent changes in the original structure occur very often in a localised region such as a highly conducting filament that might extend all or part of the way through the device. The formation of such a filament in the forming process depends largely on the structure and quality of the thin film. It can be created by crystallisation of the amorphous film [69], stoichiometric changes [70], diffusion of electrode material into the film [71], or ionisation of deep traps [72]. Details of voltage-biased forming process in a-Si:H memory devices will be described further in detail in § 4.2.

4.1.2 a-Si:H memory devices.

The first reported a-Si:H memory device structure consisted of metal-p^+ni-metal layers deposited on conducting stainless-steel substrates, where i, n, and p^+ denote intrinsic, n-type, and heavily doped p^+-type a-Si:H layers respectively. After deposition of the a-Si:H layers using an RF glow-discharge technique, thin film gold (Au) or aluminium (Al) dots were deposited onto the surface of the specimen for the top contact [21,22]. After electro-forming, the p^+ni structure usually exhibits extremely fast transition times ($100ns$ or less for both the WRITE or ERASE operations), non-volatile, and polarity dependent switching properties, analogous to crystalline volatile (threshold) metal-insulator-semiconductor-semiconductor (MISS) devices [73]. When switched to a resistive OFF-state, the current was found to scale with device area. The metal-p^+-metal structures developed later retain the main features shown in p^+ni structures. In addition, this type of device structure shows other unique characteristics in switching operations [10, 74]. Once the device reaches its first non-volatile ON-state after forming, all subsequent switching operations

can be performed with a low bias voltage pulses (i.e $1-5V$, $10-100ns$). In particular, in some circumstances (eg. with vanadium as the top contact), the switching between ON-state and OFF-state can be varied through a continuous range of intermediate resistance states, which is a feature of analogue switching, as shown Fig. 4.2. In the case of WRITE pulses, a positive bias is

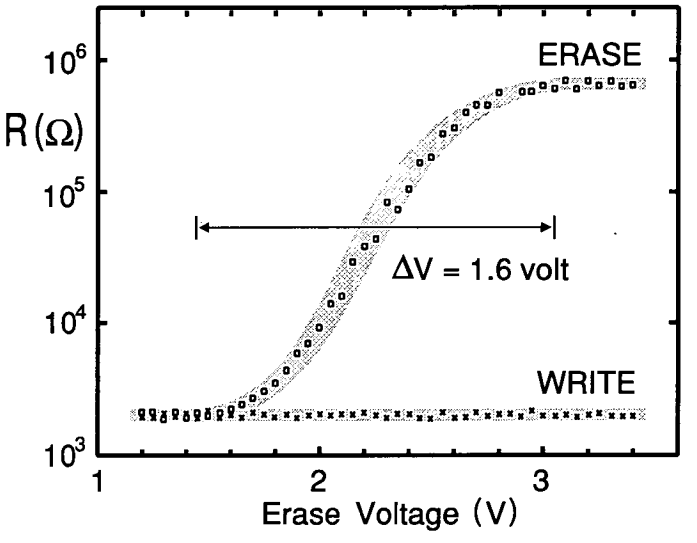


Figure 4.2: Analogue switching characteristic in a Cr-p^+-V memory device (from Owen *et al* [7]).

applied to the Cr track (bottom contact), whereas ERASE pulses have the opposite polarity. The sample was first switched to an ON state ($R_{ON}= 2 \times 10^3\Omega$) and then a series of alternating WRITE and ERASE pulses were applied. The WRITE pulses were kept at a constant magnitude of 3.4V but the ERASE pulses were incremented by 0.05V steps from 1.2 to 3.4V after each WRITE pulse. It can be seen from Fig.4.2 that the sample resistance changes in an analogue manner as the magnitude of the ERASE pulse increases, that is, the difference between R_{ON} and R_{OFF} is a function of the magnitude of the ERASE pulses. A voltage range of ΔV (ERASE) = 1.6V resulted in a change in resistance from $R \sim 2 \times 10^3\Omega$ to $R \sim 6 \times 10^5\Omega$. The reverse operation, i.e. changing the resistance from OFF-state into an ON-state, can also be readily carried out through maintaining a constant ERASE voltage and increasing the voltage of WRITE pulse. By selecting the correct polarity and magnitude of

the WRITE and ERASE pulses the device will switch between any two resistance states within the range from about 1 $k\Omega$ to 1 $M\Omega$. For all devices with a V (vanadium) top contact, the value of ΔV ranges from $1.5 - 1.6V$ for both the WRITE and ERASE operation but ΔV is different if other metals are used as the top contact material. The effect of the top contact is described in § 4.1.3.

The I-V characteristics of analogue memory-resistance states at room temperature can be described by a simple empirical nonlinear relationship:

$$I = C_1 V + C_2 V^n \tag{4.1}$$

where C_1 and C_2 are constants and the exponent n increases with the low bias resistance. Conduction is found to be thermally activated in most resistance states, but the activation energy decreases as the resistance of the memory state reduces, as shown in Fig. 4.3 [8]. The resistance follows a well-defined

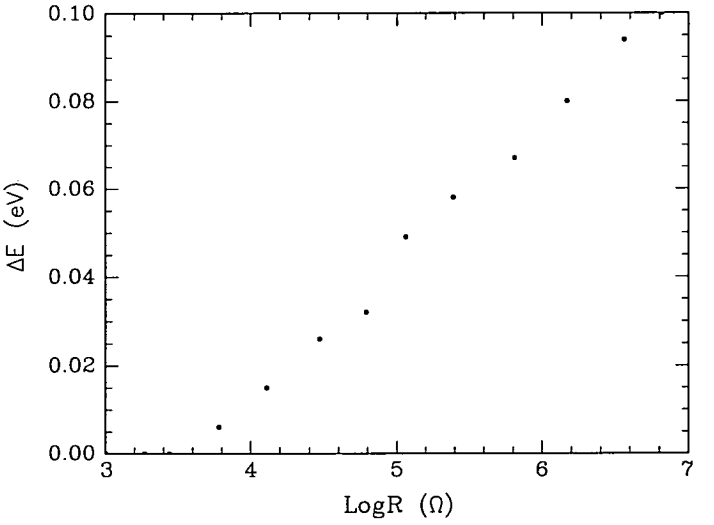


Figure 4.3: Activation energy *vs.* memory resistance (from Rose *et al* [8]).

functional form of $exp(\Delta E/k_B T)$, becoming less temperature-dependent as ΔE approaches very low values, for low resistance ON-states. This may result from a change in current transport mechanisms.

The dynamic resistance, (dV/dI), of formed devices at biases less than $100mV$ for both ON- and OFF-states exhibits a resistance peak centered around zero volts, which increases with decreasing temperature, as shown in Fig. 4.4 [9]

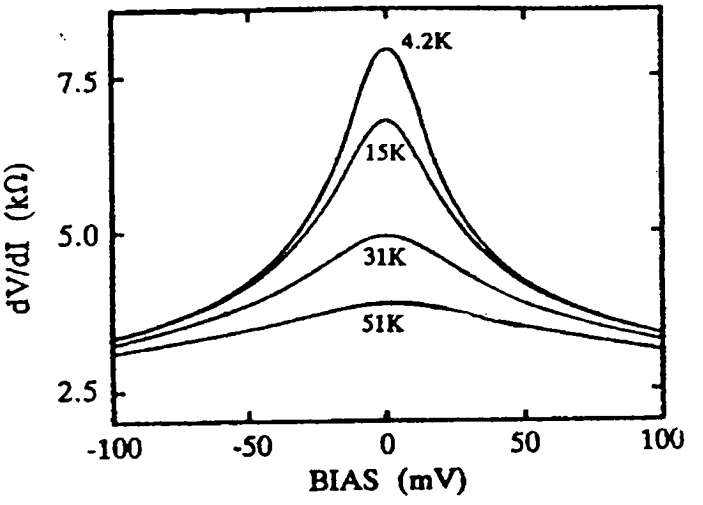


Figure 4.4: Dynamic resistance (dV/dI) *vs.* bias at different temperatures for a formed sample with Cr top contact in a memory ON-state (from Gage *et al* [9]).

As discussed in *Chapter* 5, this characteristic of (dV/dI) implies that the filament in formed devices may contain small metal islands embedded in an a-Si:H matrix, with electron transport dominated by an activated tunnelling via the embedded metallic islands.

4.1.3 Effect of the top contact on switching.

Experiments have revealed that the top metal contact plays a crucial role in determining the type of memory-switching phenomena, in terms of the voltage range ΔV. This is shown in the Table 4.1. Devices with Mo and Pd as top metal contacts show a volatile memory-switching effect, while those with Au, Cu, or Ti show a no switching, or at best, unstable switching characteristics. In addition, among those devices showing non-volatile switching, the switching window ΔV, thus the switching type (either digital or analogue) is dependent on the different top contact materials.

Metal	$\Delta V(V)$	Switching Characteristics
Ag,Al	< 0.1	Digital, non-volatile
Cr	0.2	Digital, non-volatile
Mn, Fe	~ 0.5	Digital, non-volatile
Ti	-	Unstable switching
Au, Cu	-	No switching
W	~ 0.1	Analogue, non-volatile
V	1.8	Analogue, non-volatile
Ni, Co	2.0	Analogue, non-volatile
Mo, Pd	2.0	Analogue, volatile

Table 4.1: Effect of top metallisation on switching behaviour (from Hajto *et al* [20]).

4.1.4 Memory mechanisms.

Extensive efforts have been made to explain the origin of the switching process. Thermal and electro-thermal models [75, 76] used to explain the behaviour of the amorphous chalcogenide memories fail to explain the extremely fast WRITE and ERASE speeds in a-Si:H memory devices. For example, the WRITE operation time for the a-Si:H devices is $\sim 10^{-8}s$, that is five orders of magnitude faster than in chalcogenide devices ($\sim 10^{-3}s$). Moreover, the forming, WRITE and ERASE operations for the a-Si:H memories are generally polarity dependent. The "punch-through" model [73] explains well the threshold (volatile) switching behaviour of *crystalline*-silicon MISS structures, i.e. the current instabilities and fast polarity-dependence, *etc*, but it cannot account for the feature of non-volatile memory behaviour.

Based on the analysis of ballistic electron transport occurring in Cr/p^+a-Si:H/V devices, Hajto *et al* proposed an idealized model to account for the memory mechanism in a-Si:H switching devices, as illustrated in Fig. 4.5. The observed resistance of formed structures is determined by contribution from either highly conducting inclusions (refered to as material A, with resistance R_A) or a "gap" region between metal inclusions (referred to as material B

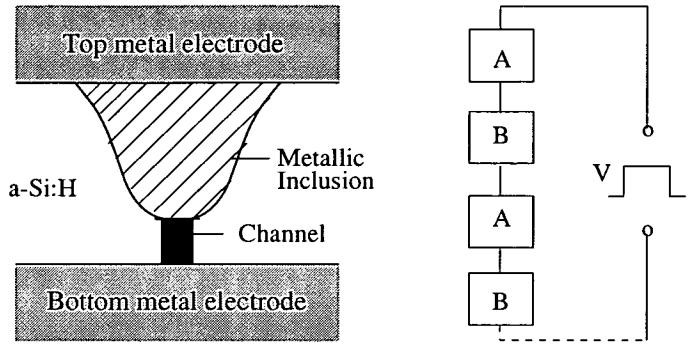


Figure 4.5: (a) Single permenant inclusion and conducting channel; (b) one-dimensional arrangement of the conducting filament (from Hajto *et al* [10]).

with a resistance R_B). In the ON state, $R_B < R_A$, so that the measured electrical properties are those related to material A, i.e.an ohmic I-V characteristic and usually a small thermal activation energy. In the OFF state, $R_A < R_B$, and inter-island (or metallic inclusion) tunnelling dominates. At low bias ($V << \Phi$) and constant temperature, the current density is expressed by

$$J = cVexp(-s\Phi^{\frac{1}{2}}) \tag{4.2}$$

or, the isothermal resistance in the B-like region is

$$R = c'exp(s\Phi^{\frac{1}{2}}) \tag{4.3}$$

where c' is a constant, s (in Å) and the Φ (in eV) are the spacing between the metallic inclusions and barrier height of the inclusion, respectively. According to Eq.(4.3), a small change in either s or Φ could lead to a change in R of many orders of magnitude. This tunnelling model assumes the existence of metallic inclusions in the conducting filament and correlates the switching with structural parameters like s. However, it does not explain the systematic dependence of device resistance on the magnitude and polarity of the switching voltages as shown in Fig.4.2.

Jafar and Haneman [24] recently presented a model in which the filament, similar to Fig.4.5(a), consists of two parts after the forming process. One is the metal-containing region resulting from the diffusion of the top metal. The other (channel region) is the remaining a-Si:H matrix of relatively high resistance. To account for the polarity dependence during switching, Jafar and Haneman assume that the metallic inclusions are positively charged, and move slightly under an applied electric field. This is equivalent to the length of the remaining a-Si:H changing by a amount Δl, and thus the a-Si:H resistance changes by ΔR. They then showed that a reasonable relationship between ΔR and Δl can be obtained by combining the microstructure of the filament with other observed terms, i.e., the OFF-ON transition time. According to this model some of the main features of a-Si:H memories, such as the polarity dependence, fast switching, and so on, can be explained qualitatively, but it does not explain the long retention of the memory states or the non-volatility.

In summary, there is no consistent model which can explain the overall characteristics involved in the switching process.

4.2 Voltage-biased forming process in a-Si:H switching devices.

4.2.1 Change in electrical properties.

The different a-Si:H switching structures described above have different forming characteristics. In the case of the metal-p^+ni-metal structures, a current instability phenomena as shown in Fig. 4.6, has been observed in unformed states. A displacement current occurs on applying a voltage pulse (the p^+ layer is positively biased). Some time t_d after the voltage pulse is first applied, the current rises rapidly to a maximum value I_{max}, and then decays. The onset time t_d depends on the pulse height V and temperature. Forming occurs when V approaching the critical voltage V_F (the forming voltage, typically $20-30V$ at room temperature). The high resistance of the devices ($10^8-10^9\Omega$) reduces

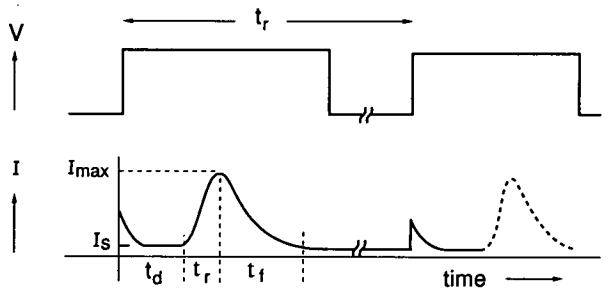


Figure 4.6: Current instability in metal-p^+ni structure during voltage-biased forming (from Choi [11]).

dramatically to a low value of $\sim 10^3\Omega$, that is the ON-state. Following this first transition, subsequent OFF-to-ON transitions occur at relatively low bias. On the other hand metal-p^+-metal structures can be formed at a lower pulsed voltage bias (typically $14V$ with a pulse duration of $300nsec$). In addition, the device resistance can be lowered gradually by applying voltage levels of progressively increasing magnitude. No sudden change of the current or voltage signal can be detected when the sample is biased with a voltage pulse until the voltage reaches a critical value (the forming voltage, $\sim 14V$), at which the device resistance drops from $\sim 10^6\Omega$ to $10^4 - 10^3\Omega$, the memory ON-state. This is shown in Fig. 4.7.

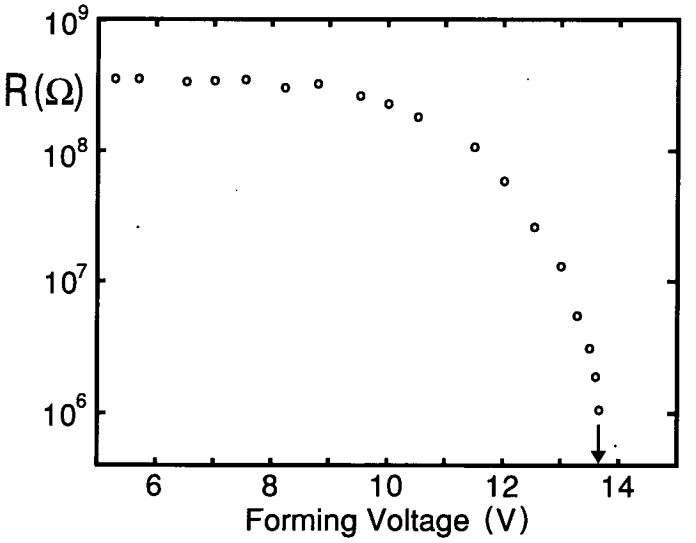


Figure 4.7: Change in device resistance of a-Si:H metal-p^+-metal structures with forming voltage (from Hajto *et al* [10]).

4.2.2 Change in original microstructure of a-Si:H.

As in other amorphous thin film structures, electro-forming in a-Si:H devices causes a substantial change in the original uniform microstructure. Much evidence has emerged that this irreversible structural modification is localised in a small region many times smaller than the original device area, accompanied by the formation of a highly conductive filament. The evidence includes experiments on the ON-state resistance as a function of area (R_{ON} is independent of area [22]), thermal imaging techniques with liquid crystals [22], the observation of current-controlled-negative-differential-resistance (CCNDR) [26], and by direct observation with a scanning electron microscope combined with microanalysis (SEM and EDX) [8]. The latter indicates that the formation of the current filament is associated with diffusion of the top metal contact into the amorphous silicon. This has been confirmed recently by Auger-electron-spectroscopy (AES) analysis [24]. Moreover, the dynamic resistances (dV/dI) of formed devices using Cr, Al, Fe, or Au as the top electrode show zero-bias resistance peaks at low temperature, similar to the behaviour observed in tunnelling junctions containing metallic particles embedded in insulating materials. Early experimental observations from thermal imaging [22] suggested that forming occurs at very low energy ($< 10^{-9}J$) and there was only a small rise in temperature as a result of applying electrical power to the pore. However, Gage argued that the experimental techniques used may have limitations in determining the real temperature increase in the filament during forming and thus the conclusion made above may not be true [12]. He modelled the internal temperature change for an ideal electrical insulator. Fig. 4.8 shows the simulation results. When applying a voltage, current passes through the device from top to bottom. The increase in temperature can be calculated from the net effect of Joule heating caused by the current in the device and the heat loss across the external surface of the insulator. The internal temperature always increases on applying a voltage pulse and then remains unchanged after a period of time. The enhancement of the temperature also depends on the

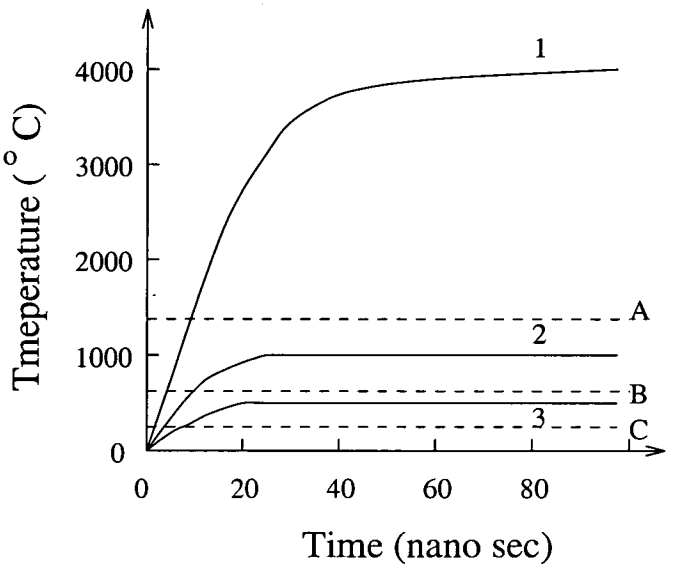


Figure 4.8: Simulation results for an ideal insulator, where A, B, and C indicate the temperature for melting, crystallisation and dehydrogenation of amorphous silicon, respectively. Curve 1, 2, and 3 represent the temperature increase for the filament with dimension of $0.3\mu m$ $(15V)$, $1\mu m$ $(15V)$, and $1\mu m$ $(10V)$ respectively (from Gage [12]).

device area. The smaller the area, the larger the increase in temperature. For the a-Si:H memory devices, this model predicts that the temperature would reach and even surpass the temperatures for dehydrogenation $(300 - 600°C)$ and crystallisation $(> 640°C)$ if it is assumed that the diameter of the filament is less than $1\mu m$. For even smaller filaments, the internal temperature could be greater than the silicon melting temperature $(1414°C)$.

Jafar and Haneman made an attempt to measure the local high temperature using an $InSb$ detector for $Cr - p^+ - Ag$ devices [23]. The devices used were deposited on a sapphire substrate with Cr bottom contacts. The infrared heat signal passes through the transparent substrate and is sensed by the detector. In this way Jafar and Haneman measured the local temperature resulting from the heating during forming and found it to be as high as $\sim 1100K$. The true forming temperature, according to their estimation, will be higher than the recorded temperature if the fact that the heated area occurs in the top electrode region is taken into account. Hence there is a temperature difference between this area and the bottom electrode (Cr). Jafar and Haneman concluded that

it is this local heating that causes the diffusion of the top electrode material (e.g.vanadium) into the a-Si:H host network.

It is likely that the high temperature drives the diffusion of the top vanadium electrode into the a-Si:H matrix. Other effects related to the local high temperature could be the loss of hydrogen, micro/poly-crystallisation of the amorphous silicon, and the formation of alloy materials such as vanadium silicides and even, possibly, borides, oxides, and hydrides. For example, Tu *et al* found that VSi_2 forms at temperatures from 600 to 1000°C [77]. Schutz and Testardi also observed that V_3Si forms between V and the boron-doped a-Si:H films by plasma deposition when the annealing temperature is over 800°C [78]. Vanadium can also react with oxgyen to form a large number of oxides, such as V_2O_5, VO_2, and V_2O_3, *etc.* [79–81]. Interstitial hydrogen atoms can exist in vanadium and causes remarkable changes in the electronic structure of vanadium [82,83]. All these materials or their mixtures contribute to the creation of the filament, which is significantly different from the original a-Si:H material.

4.3 Current stress in other a-Si:H thin film structures.

When biased with constant current instead of a voltage pulse, a-Si:H diodes exhibit features different from those mentioned above. Street *et al* investigated

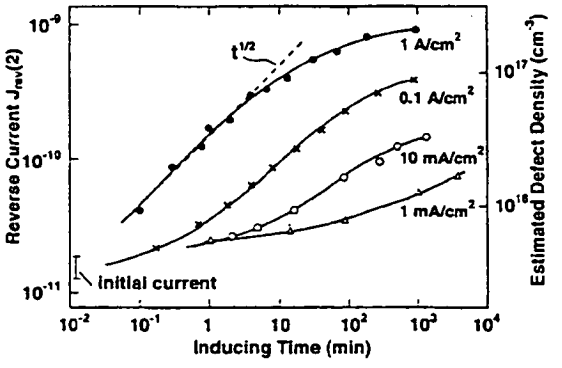


Figure 4.9: Time dependence of the current-induced defect density under different generation conditions, measured at room temperature. For comparison, the light-induced defect density is also illustrated. The right axis is the estimated defect density (from Street [13]).

defect creation in a-Si:H $p-i-n$ diodes. The reverse current in such devices is dominated by the thermal generation current [13]. When applying a forward bias current to the diode, defects are created, evidenced by an increase in reverse current which is proportional to the midgap density of states. This is shown in Fig. 4.9. The defect density increases with the time of application of the forward current bias, reaching saturation at sufficiently long times. With increasing current bias, the defect density approaches a $t^{1/2}$ time dependence before saturation occurs. In addition, the dependence on current bias is roughly ${J_F}^{1.5}$. Therefore, an empirical relation for the above defect creation process is,

$$(N_D - N_{D0}) \approx const.t^{0.5}{J_F}^{1.5}f(t) \tag{4.4}$$

where N_{D0} and N_D are the defect densities before and after stressing, J_F is the forward stress current, and $f(t)$ describes the saturation. The sub-linear time dependence is similar to the light-induced defect densities, where the defect creation exhibits a $t^{1/3}$ time dependence (see § 2.4). However, since the precise time dependence of hole concentration is unknown, the kinetics for the current-induced defect creation may differ. Moreover, as the current-induced defect creation is performed under conditions of constant current, so that the electron concentration does not decrease, the stretched exponential kinetics based on a model that depends on the concentration of electrons may also not be applicable. Shannon *et al* [67] and later Nieuwesteeg *et al* [14] observed similar defect creation to that in a-Si:H $p-i-n$ diodes when they applied a dc current bias to a-SiNx:H metal-semiconductor-metal (MSM in short) diodes [14, 67]. The current density in such a MSM structure is determined by thermionic-field emission of electrons through a reverse biased Schottky barrier [5, 67]. When stressed with a dc bias, the current (or current density) usually exhibits a reduction. This change in I-V characteristics is described in terms of a voltage shift ΔV, where ΔV is defined as the voltage change required to maintain a constant current. Fig. 4.10 shows the change of ΔV

with stress time. It is seen that ΔV exhibits a very similar time dependence

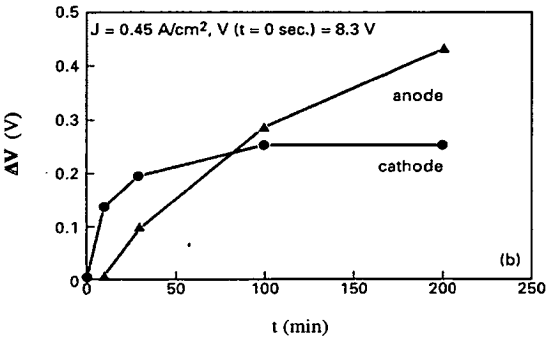


Figure 4.10: Change in voltage shift ΔV with stress time. The solid triangles and circles represent the different stress conditions according to the polarity used during the stress (from Nieuwesteeg *et al* [14]).

to that shown in Fig.4.9. Analysis shows that ΔV is proportional to the space charge density in the a-SiNx:H bulk. Therefore, the above change reflects the time dependence of defect density creation during current stress. The mechanism of defect creation can still be described by electron-hole recombination, similar to the mechanism proposed by Stutzmann *et al* [54]. The rate of defect creation is determined by

$$\frac{dN_D}{dt} = Kpn \tag{4.5}$$

where K is a constant, and n and p are the concentration of electrons and holes respectively. For the hole concentration p, Shannon assumed that the supply of holes is modified by the electron current flowing into the anode because of the very large kinetic energy of the electrons entering the anode, induced by both the high field at the anode and the gain of extra energy $q\phi_a$ (about $0.9eV$ in a-SiNx:H diodes). This supposition leads to a sublinear dependence of ΔV on time under constant-current stress J, $\Delta V \propto \sqrt{t}$.

Chapter 5

Properties of Granular Metal Films.

Granular metal films are two dimensional composites containing metal particles embedded in an insulator matrix. This chapter describes some of the main electronic properties of granular metal films, such as activated tunnelling, the Coulomb blockade effect in small tunnelling junction and metal-non metal transition phenomena, which are relevant to the subject of this thesis.

5.1 Activated tunnelling in granular metal films.

The tunnelling concept arises from the quantum-theory prediction that an initial state, prepared in one classically allowed region of configuration space, has a nonzero probability of penetrating through a classically forbidden region into a second classically allowed region. In metal-insulator-metal systems, when an electron tunnels between two electrodes whose Fermi levels are fixed, no electrostatic work has to be done since the positive charge left behind is immediately neutralised and no energy is added to the system. In the case of granular films, however, the tunnelling effects have a behaviour different from that in metal-insulator-metal system. When an electron is removed from one initially neutral island and is added to another some distance removed, energy is added to the system, hence resulting in an increase in the system energy. This energy will be of the order of magnitude (q^2/r), where r is the average linear dimension of the particle [84,85]. Fig. 5.1 is the relevant energy band

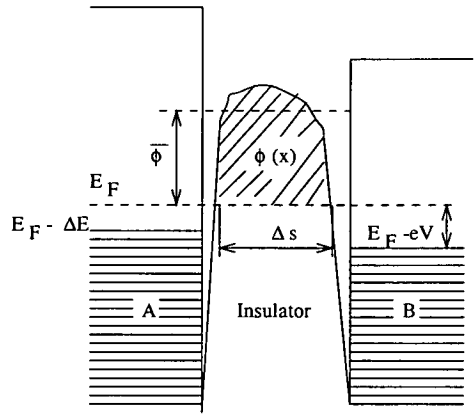


Figure 5.1: The energy diagram for electron tunnelling from metal island A to B. ΔE is the energy required for an electron to transfer from A to B.

diagram, where ΔE represents the energy needed for the transfer of an electron.

According to Neugebauer and Webb, only electrons or holes excited to states of at least that energy (q^2/r) above the Fermi level will be able to tunnel from an originally neutral metal particle to another [86]. This model predicts that the conductivity of a thin granular film should depend exponentially on reciprocal temperature over a reasonably large temperature and conductance interval; the films should display ohmic behaviour, at least in the limit of small applied electric field; and there should be a marked dependence of the activation energy for conduction on particle size. In addition, the activated tunnelling mechanism was combined with other conduction mechanisms to explain experimental data. For example, Feldman [15] studied partially continuous films exhibiting a transition of the temperature coefficient (TCR) from positive to negative with decreasing temperature, as shown in Fig. 5.2. The resistivity of the films is that of a metal bulk in series with the gap resistivity between metal grains and thus can be expressed by an equation of form

$$\rho = \rho_0[1 + \alpha_T(T - 273)] + Cexp(\vartheta/k_BT) \tag{5.1}$$

The transition temperature T_{min} can obtained from $(d\rho/dT = 0)$. Therefore,

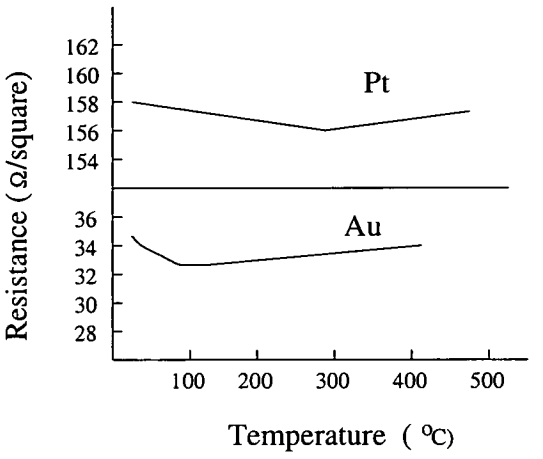


Figure 5.2: Resistance versus temperature for partially continuous films (from Feldman [15]).

above T_{min} the conduction is metallic, while below T_{min} activated conductivity dominates.

The ac characteristics of granular metal films have been studied by many researchers. Hirsch and Baziah [87] measured the ac conductance of thin layers of pure nickel and silver and used a simple circuit to represent such discontinuous films. In this model metal islands are represented by a resistor connected in series with a capacitor and resistor, these two being connected in parallel and representing the intergranular capacitance and conductance respectively. Hirsch and Baziah found that the ac conductance $\sigma(\omega)$ of the films increases with the square of the frequency ω, $\sigma(\omega) \propto \omega^2$. However, Tick and Fehlner [88], and later Morris [89] found that the frequency dependence of the films they studied obeys the relation: $\sigma(\omega) \propto \omega^{0.9-1}$, which they attributed to hopping conduction occurring between the islands. Morris [90] also studied thin films deposited asymmetrically and observed strongly polarity-dependent resistances, and "pseudo-inductive" effects at low frequencies.

Generally, a structure in which metallic grains are separated by small spacings is electrically equivalent to a series of capacitors, and consequently its ac impedance is less than the dc value. When temperature is reduced, the difference between ac and dc will become progressively larger, since the dc resistance

of the granular films increases rapidly with decreasing temperature. Fig. 5.3 shows experimental results obtained by Offret and Vodar [16] for platinum on

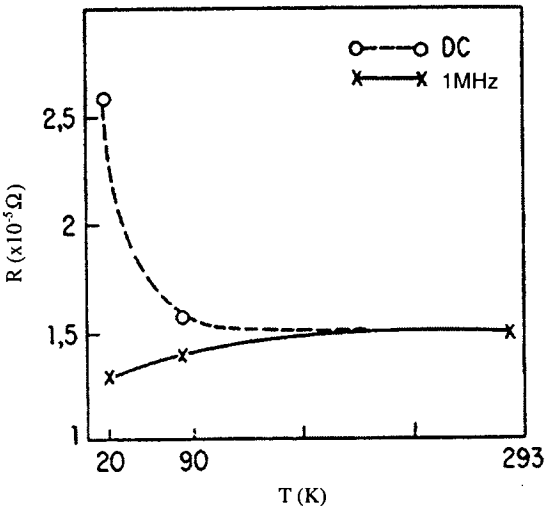


Figure 5.3: Comparison of dc and high-frequency resistance of a discontinuous film (from Offret *et al* [16]).

Pyrex. At low temperatures the ac impedance (at $1MHz$) shows a positive temperature coefficient, reflecting the TCR of the metallic grains themselves, due to the spaces between the grains being effectively short-circuited by the alternating current, while the dc resistance shows a negative temperature-dependence in the same temperature range. In the high temperature range, however, the dc current is large enough for the resistance to be dominated by that of the grains, so that the dc and ac resistance merge into the same curve.

When metallic particles are small enough, the Coulomb charging energy will become comparable with the thermal energy k_BT. An important phenomena known as the Coulomb blockade effect occurs in such ultrasmall junctions. Giaever and Zeller [17,91] first observed this effect in a study of $Al-Al_2O_3-Al$ junctions containing fine Sn particles in the oxide, as seen in Fig. 5.4(a). They noticed that when particles are in the normal (metal) state, all junctions show a dynamic resistance maximum at zero bias, as shown in Fig. 5.4(b). This effect may be present even at room temperature but it increases with decreasing temperature. At low temperatures the zero-bias resistance is inversely propor-

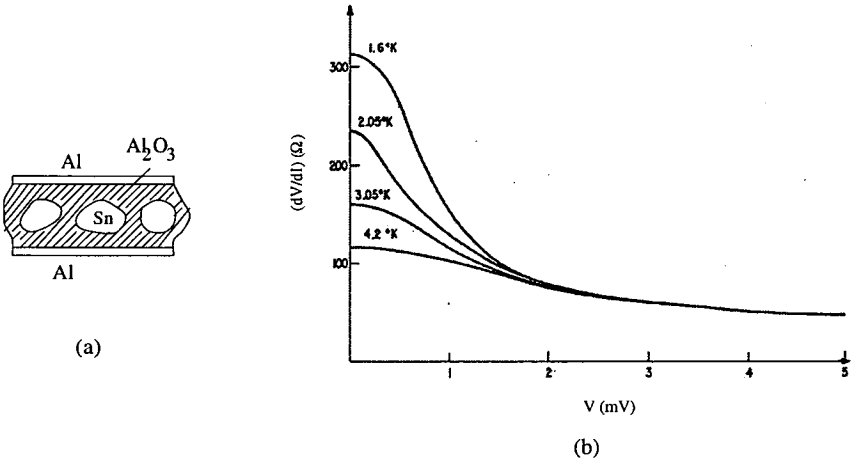


Figure 5.4: (a) The tunnelling structure; and (b) dynamic resistance-versus-voltage characteristic. The average particle radius is $\sim 150\mathring{A}$ (from Giaever *et al* [17]).

tional to temperature while the resistance at voltages $V \ll (k_B T/e)$ is largely temperature-independent.

Kulik and Shekhter [92], and later Averin and Likharev [93,94] analysed quantitatively these experimental results using a more rigorous quantum-mechanical method, and confirmed that the anomaly is due to the Coulomb blockade effect. Averin and Likharev predicted correlated single charge transfer in tunnel junctions with extremely small capacitances. They analysed a single junction driven by a current source [95,96], and found that if the temperature satisfies the relationship

$$T \ll T_0, \qquad T_0 \equiv \frac{e^2}{2k_B C_m} \tag{5.2}$$

where C_m is the junction capacitance, then tunnelling of even a single electron would lead to an increase of the charging energy $(q^2/2C_m)$. Thus no tunnelling current would occur. This is the "Coulomb blockade", which causes the accumulation of electrical charges supplied by the bias current. Averin and Likharev's analysis also showed that the transference of a single electron drastically reduces the possibility that other electrons may tunnel at the same time, which suggests that the tunnelling event between two electrons is correl-

ated.

5.2 Metal-non metal transitions in granular metal films.

The metal-non metal transition in granular metal films usually occurs when the volume fraction of the metal particles reaches a critical volume p_c. The conductivity undergoes a transition at p_c from activated tunnelling to metallic conduction, and the dielectric constant of the composite usually exhibits a notable increase [97–100]. From the conduction point of view, granular metal materials can be divided into three distinct regimes as the volume fraction of one of the constituents changes.

i) Metallic regime: the overlapping metal particles form a continuum with dielectric inclusions. Electrical conduction is through the metal but the overall resistivity of the film is higher than the resistivity of pure metal. The TCR in this regime is positive, as in a metal.

ii) Dielectric regime: the dielectric materials form a continuum with metallic inclusions. Electrical conduction is by thermally activated tunnelling between the metal islands with an additional contribution to the current occurring solely through 'leakage' in the dielectric. The TCR is negative.

iii) Transition regime: the regime in which a structural inversion between the metallic and dielectric regimes takes place. Electrical conduction takes place by percolation of electrons along the metallic maze and by tunnelling between island metal particles. The TCR is negative.

The anomalous changes in electrical properties (i.e. dc dielectric constant) near a metal-non metal transition has been described in terms of either the Maxwell-Garnet (MG) or a percolation approaches. The MG approach mainly deals with the composites where the dispersions (e.g.metallic particles in a metal-insulator mixture) are usually regarded as an idealised array with equal size and are regularly spaced inside the host medium [101–105]. The percol-

ation approach investigates structures with a random nature as observed in practice, particularly the critical behaviour of the effective dielectric constant (or conductivity) near the threshold volume fraction at which a metal-non metal transition occurs [106–108]. The conducting exponent (or called critical index) in percolation problems is found to be universal. It is the same for lattice and continuum systems, and also the same no matter what kind of physical parameter (composite, temperature, or light intensity) causes the increase of the metallic component and eventually results in the metal-non metal transition.

If p_c is the percolation threshold for component 1, above which that component 1 forms an infinite extended conducting path, then near the MNM transition, the effective dielectric constant can be expressed by the following formula [109,110]:

$$\epsilon_{eff} = \epsilon_h \mid \frac{p - p_c}{p_c} \mid^{-q} \tag{5.3}$$

where q is the critical exponent, $q \sim 0.75$ and ~ 1.3 for a three-dimensional and two-dimensional heterogeneous conductor-dielectric binary composite respectively, ϵ_h is the dielectric constant of the host material, p and p_c are volume fractions of the particles and the threshold (percolation volume) respectively. Note that q depends only on the dimensionality of the composite, but not on its local microstructure and the type of the percolation problem. The percolation theory predicts that near p_c the ac conductivity $\sigma(\omega, p)$ and dielectric constant $\epsilon(\omega, p)$ of a random mixture should obey a power-law behaviour, and the exponents x (for $\sigma(\omega, p_c)$) y (for $\epsilon(\omega, p_c)$) should satisfy $(x + y = 1)$ [98].

Chapter 6

Experimental Details.

6.1 Device Structure and Preparation.

6.1.1 Device structures.

The devices used for this work are Cr-p^+hydrogenated amorphous silicon (a-Si:H)-V sandwich structures configured as shown schematically in Fig. 6.1, where (a) and (b) represent the cross-section and plan view, respectively. The

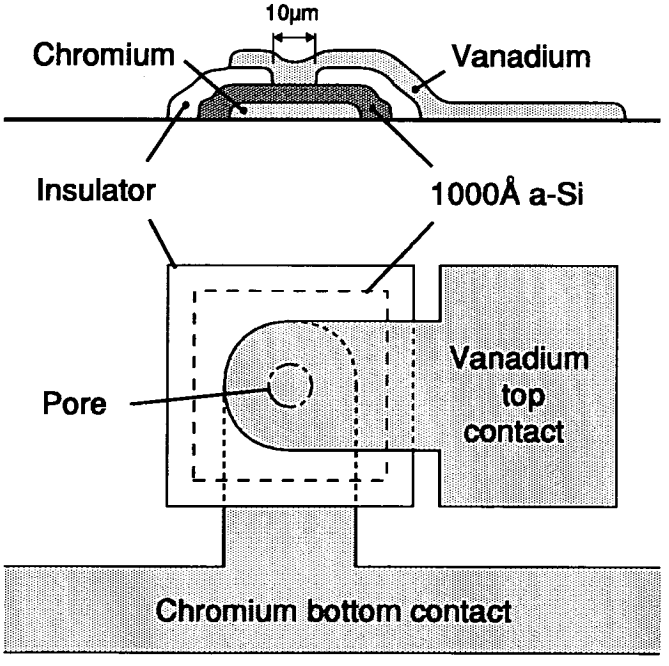


Figure 6.1: Schematic diagram of the structure Cr-p^+a-Si:H-V devices.

p^+-a-Si:H layer, with a thickness ranging from 500$\AA$ to 1000$\AA$, is prepared by the RF-glow-discharge decomposition of silane (SiH_4) containing typically

$10^3 - 10^4$ *ppm* by volume of B_2H_6, with the contact area defined by a 10-μm diameter pore in an insulating layer. The top (V) and bottom (Cr) metal electrodes are prepared by sputtering or vacuum evaporation. The device is usually deposited on an oxided crystalline silicon wafer. An insulating substrate of Corning 7059 glass is used in some cases.

Compared with the "dot" devices used in early a-Si:H memories [21], which normally had a relatively large diameter ($\geq 0.5mm$) defined by a dot or disc thin film top contact, this pore structure represents a major improvement in the study of a-Si:H switching. Several advantages can be gained from the reduced size of the device (typically $10\mu m$-diameter or less). For example, it reduces the potential damage induced by large currents through the device in the OFF-state. The current is usually found to scale with device area. If the device diameter is relatively large, the capacitive energy stored is also very large at the instant of switching.

6.1.2 Preparation.

All the Cr-p^+-a-Si:H-V devices used in this study were prepared at the Carnegie Laboratory of the Department of Applied Physics and Electronics & Manufacturing Engineering, University of Dundee. Fig. 6.2 illustrates the diode configuration of the deposition system. During deposition, silane SiH_4 (diluted with hydrogen or other gases, or mixed with certain doping gases like B_2H_6) is admitted into the chamber through the gas inlet, controlled by the flow controllers, and is decomposed in the plasma area confined between the substrate and the electrode connected to the RF power source. The typical frequency of the RF power is $13.56MHz$. For doped a-Si:H, the doping ratio of B_2H_6/SiH_4 is precisely determined by the flow controllers, or pre-determined using a gas-mixing tube before the gas ($SiH_4 + B_2H_6$) is admitted into the chamber. One of the main advantages of plasma deposition is that although the temperature within the reaction region is only several hundreds of Kelvin,

the electron temperature T_e can be as high as $10^4\ K$ when the gas pressure is at $0.1 - 1\ Torr$, and the density of electrons also is high: up to $10^{12}\ cm^{-3}$.

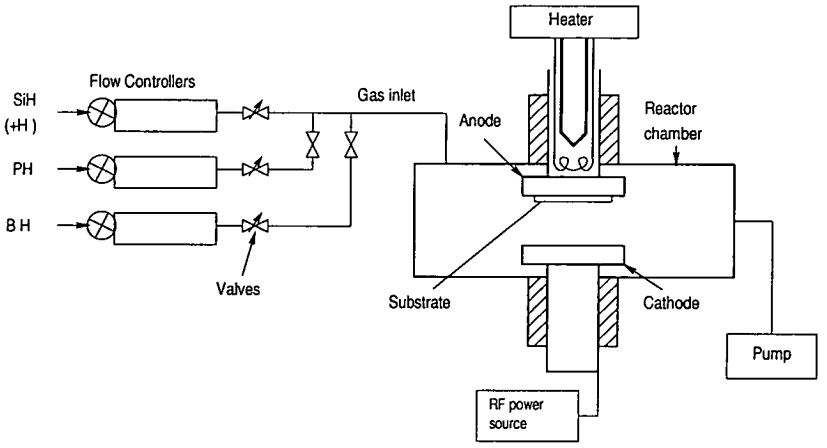


Figure 6.2: Schematic diagram of the capacitive-coupled glow discharge deposition system for the preparation of a-Si:H.

The energetic electrons are able to excite, decompose, or ionise the SiH_4 gas molecules, producing numerous ions (i.e. $Si^+, Si_iH_j{}^+$, $i,j \geq 1$) and radicals (i.e. H, SiH_i, $i = 1 - 3$). These ions and radicals continue to react with each other during the process of diffusion to the substrate, as the mean free path of the gas molecules is $10^{-3} - 10^{-2} cm$ and is much smaller than the dimensions of the reactor. On the growing surface there exist various complicated physical-chemical reactions which have a vital effect on the structure and properties of the subsequent film. Therefore, it is important to choose the proper deposition parameters, such as RF power, substrate temperature, gas flow rate, and pressure in the reaction chamber, *etc*, for an optimum deposition process.

Table 6.1 lists the main deposition parameters for some of the devices used in this study. The activation energy of conduction is in the range of $0.18 - 0.2\,eV$ for a doping concentration $[B_2H_6]/[SiH_4]$ of $10^3 - 10^4 vppm$ [111].

Batch No.	Type	level($vppm$)	$T_s(°C)$	L (Å)
430-4	p	10^4	220	950
430-5	p	10^3	220	750
430-6	p	10^3	220	1100
430-7	p	10^4	220	1750
430-8	p	10^3	220	700
430-9	p	10^4	220	800
430-10	p	10^3	220	1200
430-11	p	10^4	220	900
430-12	p	10^4	220	900
10040-13BT	p	10^4	220	1000
10070-14BT	p	10^4	220	1000
96-9	p	10^4	275	700
New-4	p	10^3	245	945
New-6	p	10^3	245	945

Table 6.1: Preparation conditions and thickness of the p^+ layer of some batches of specimens used for this work.

6.1.3 Wiring and bonding of the samples.

The as-deposited samples are first cut into small pieces, each of which comprises $20 - 30$ of the pore devices shown in Fig.6.1. Each piece is bonded to a 24- or 28-pin package. The chip bonding diagram for a standard 28-pin package is illustrated in Fig. 6.3, where (a) is plan view and (b) a side view of the chip.

6.2 Experimental setup for current stressing and forming.

Fig. 6.4 shows the setup used initially for current-forming. A Keithley Model 224 Current Source supplies the current through the sample under test, while a Keithley Model 196 Digital Multimeter (DMM) is used for measuring the voltage change across the sample during the course of the forming.

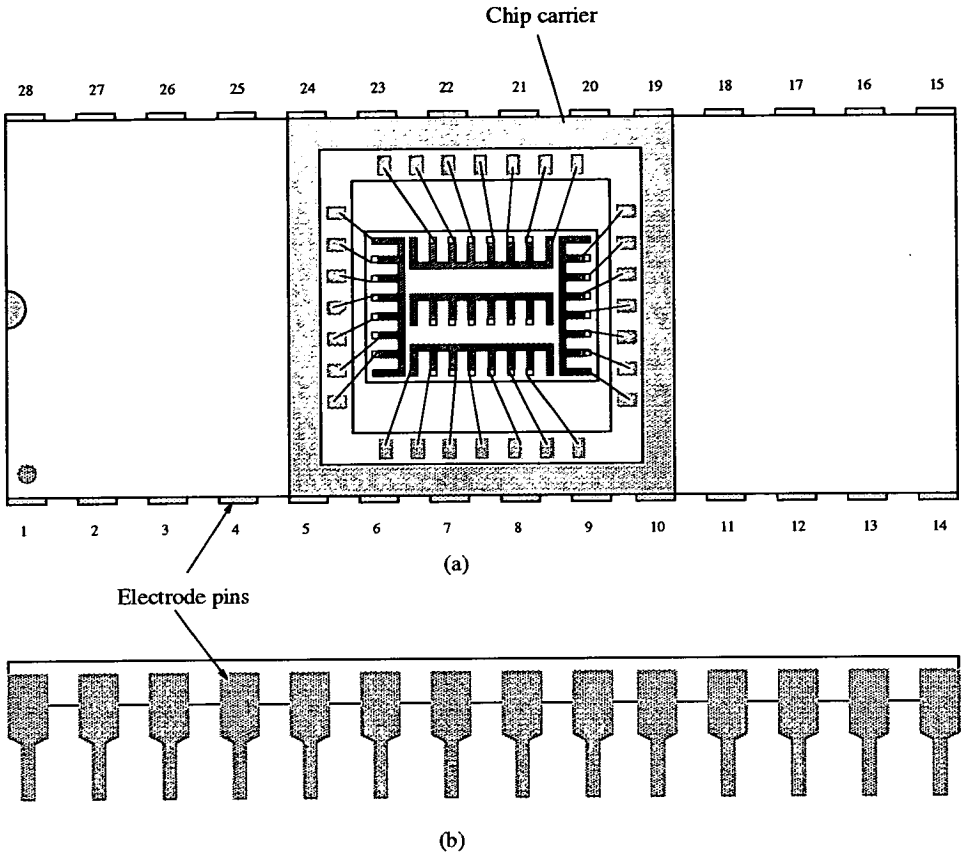


Figure 6.3: Chip bonding diagram.

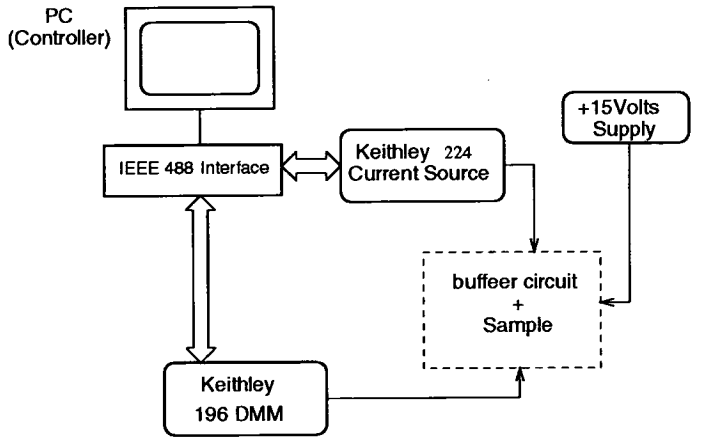


Figure 6.4: Schematic diagram of the setup for initially current forming experiments (from Scott [18]).

Due to the relatively low input impedance of these instruments (i.e. $\sim 1M\Omega$ for the DMM which is much lower than the unformed sample resistance $10^8 - 10^9\Omega$), a buffer circuit consisting of an op-amp (353 FET type) is used to buffer

the sample from the DMM. To monitor more effectively the change in voltage across the sample during stressing and forming, another testing setup as shown in Fig. 6.5 is also used. A HP4145A Semiconductor Parameter Analyser is

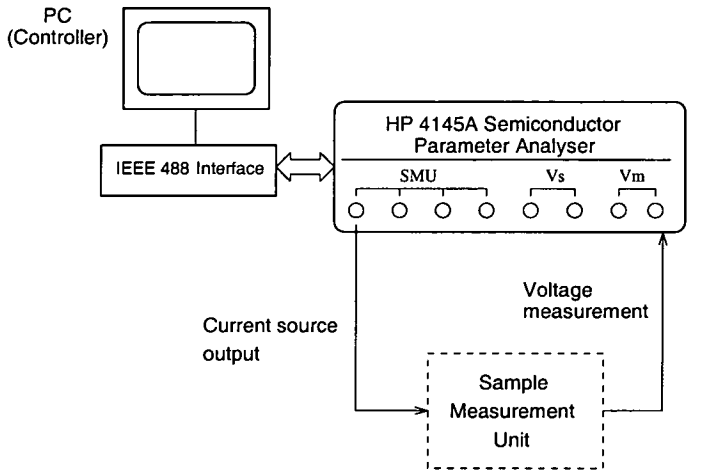


Figure 6.5: Schematic diagram of the setup for current forming experiments.

used as both current source and voltage monitor simultaneously through one Stimulus/Measurement Unit (SMU) and one voltage monitor V_m. A simplified circuit diagram of a SMU is shown in Fig. 6.6 [112]. An extra buffer circuit

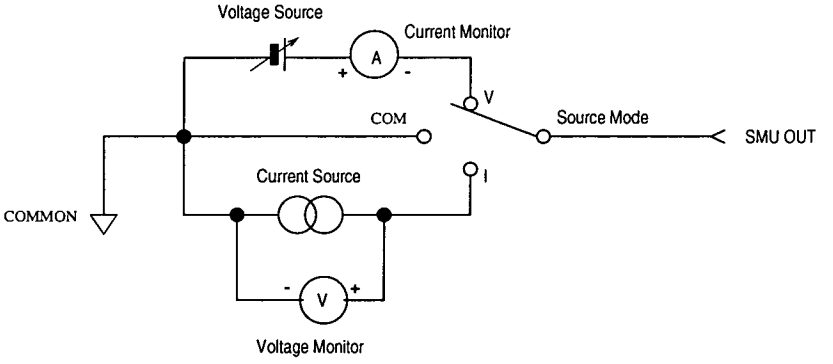


Figure 6.6: Circuit diagram of a SMU.

such as that in Fig.6.4 is no longer needed, as the input resistance of each of SMU is larger than $10^{12}\Omega$ when used as a current source. Except for the main channel used as the current source, the other channels (three SMUs and two V_s) can be swept synchronously with the main channel. The V_m channels are

used to measure the voltage change across the sample during stressing and forming. Using the HP4145A Analyser for the forming experiments simplifies the measuring circuit, and also helps to enhance the precision and stability. In addition, using the programming codes built into the instrument, experiments can be performed automatically, controlled by a PC. The output accuracy of both voltage and current sources of the HP4145A is listed in Table 6.2. In a Current Source/Voltage Measurement Mode, the resolution and accuracy of the two voltage monitors (V_m) are listed in Table 6.3.

Sources	**Range**	**Accuracy**
Voltage	$\pm 20 - \pm 100V$	$0.1\% + 0.05\% + 0.4\Omega \times I_0$
Current	$\pm 1nA - \pm 100mA$	$0.3\% - 1\% + (0.1 + 0.2 \times V_0/100)\%$

Table 6.2: Accuracy specifications in the above table are given as $\pm n\%$ of output value, $\pm n\%$ of range value. I_0 and V_0 are the output current and voltage, and 0.4Ω is the residual resistance when the instrument works in a Voltage Sources/Current Measurement Mode.

Measurement Range	**Resolution**	**Accuracy**
$\pm 2V$	$100\mu V$	0.5% of reading + $10mV$
$\pm 20V$	$1mV$	0.2% of reading + $10mV$

Table 6.3: Accuracy specification for voltage monitors.

6.3 Experimental techniques for dc and ac measurements.

A schematic diagram of the equipment for dc and ac measurements is shown in Fig. 6.7. Using the voltage source facility of the HP4145A Semiconductor Parameter Analyser, the static I-V characteristics of unformed/formed samples can be measured manually or automatically over a wide range ($V = 0 - \pm 100V$ and $\pm 1nA - \pm 100mA$). The ac characteristics of samples are measured by a Schlumberger 1260 Impedance/Gain-phase Analyzer. This instrument

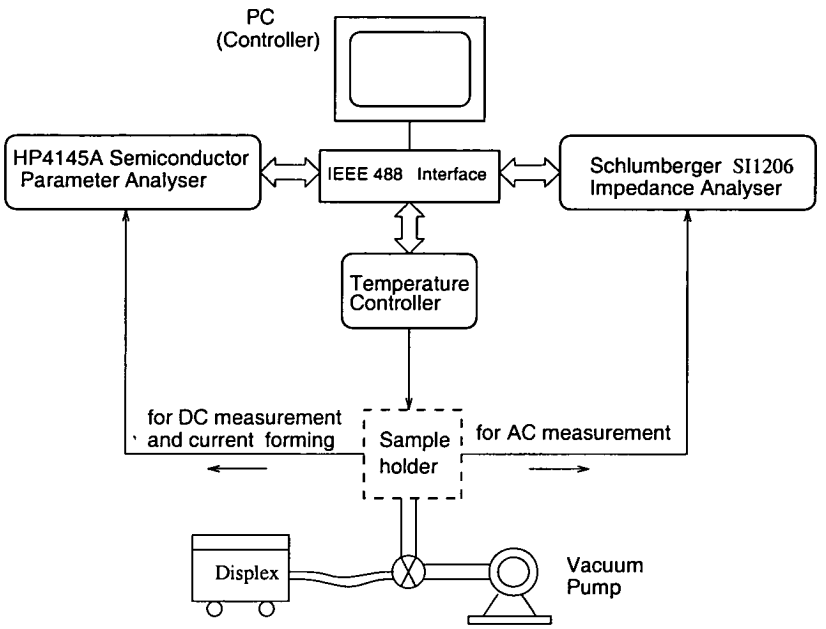


Figure 6.7: Schematic diagram of the setup for dc and ac measurements.

provides a comprehensive range of impedance and frequency response measuring facilities [113]. The measuring frequency ranges from $10\mu Hz$ to $32MHz$ with amplitude of $0-3V$, and with very low measurement error of $\pm 100ppm$ ($\pm 10ppm$ under the stabilised circumstance). Sweep measurements include 1) frequency sweeping with or without dc bias, or changing bias; 2) voltage sweeping at fixed frequency. In order to reduce the errors during frequency sweep measurements, there is a built-in nulling facility to eliminate stray capacitance. The connection between the DUT (device under test) and the instrument has a two-pair four terminal configuration, so as to minimise the effects of the leads.

For the measurement of dc and ac characteristics over a wide temperature range, a Displex Closed-Cycle Refrigeration System (Displex for short) is used. The Displex is basically a refrigerator operated by helium gas [114]. Cryogenic temperatures as low as $10K$ are achieved in the expander as the compressed helium is expanded. A heater, controlled by a LakeShore Model 330 Autotuning Temperature Controller via temperature sensors (made of $GaAlAs$ diodes), is put in the tip of the expander which gives temperature control in the range of

10 to $300K$. During measurements, the sample is fixed on the sample holder, which is covered by a vacuum shroud. The vacuum shroud is first pumped down to a rough vacuum of 1×10^{-3}torr by a rotary pump to avoid condensation, which prevents cool down. When the temperature in the expander reaches $220K$ the valve connecting the vacuum pump to the expander is closed, and the cryopump in the expander then starts work to achieve high vacuum ($\sim 10^{-5} torr$).

Chapter 7

Unstressed Devices.

7.1 Electrical properties.

7.1.1 J-V characteristics.

Fig. 7.1 shows a typical set of current density vs. voltage characteristics for as-deposited Cr/p^+a-Si:H/V devices with positive polarity applied to the V (top) electrode. Note that the current exhibits a non-saturating characteristic

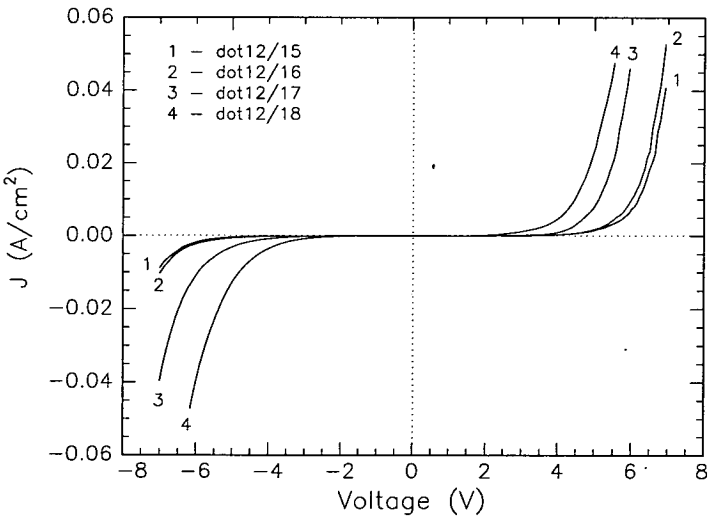


Figure 7.1: Typical J-V characteristic of the unstressed V/p^+a-Si:H specimens (samples from batch 96-9, see Table 6.1).

with increasing voltage, and it increases nearly exponentially with bias. The characteristics are almost symmetrical, in contrast to the highly asymmetric form of current density-voltage characteristics for typical diodes. The symmetry in the present case arises from the fact that the device comprises two

Schottky barriers (Cr- and V-a-Si:H respectively) back to back. For the present purposes, the forward direction is defined to be that when the V contact is positive. The slight difference in the forward and reverse directions, evident in Fig.7.1, is probably due to the different barrier heights of the two junctions (Schottky barriers). Small variations in the J-V characteristics among different specimens probably results from variation in the deposition process. The J-V characteristics suggest that current transport over the reverse-biased V/a-Si barrier does not follow a pure thermionic-emission/diffusion mechanism, which predicts saturation at larger reverse biases (note that one of the Schottky barriers is always reverse-biased) [61]. Instead, it is consistent with a transport mechanism based on the model of thermionic-field emission. As described in §3.2, tunnelling due to heavy doping causes a reduction of the effective barrier height. Moreover, an increasing reverse bias reduces the barrier width and further enhances the tunnelling probability. As a result, the device current exhibits a near-exponential increase under increasing reverse bias.

7.1.2 Temperature dependence.

The temperature dependence of the current density-voltage characteristics measured over the range of $200 - 300\,K$ is shown in Fig. 7.2. With decreasing temperature, there is a systematic reduction in device current density. The conductance G $(= I/V)$ obeys, approximately, an Arrhenius-type equation:

$$G = G_0 exp(-\frac{E_a}{kT}) \tag{7.1}$$

as illustrated in Fig. 7.3, with the reverse bias as a parameter. In the higher temperature region $(> 220K - 230K)$ there is a reasonably well defined activation energy E_a which decreases with increasing reverse bias. Below $220-230K$, the slopes of the $LogG\ vs\ (1/T)$ curves decrease almost continuously with increasing $(1/T)$ and in the range of higher biases (eg $> 1V$) the conductance becomes essentially temperature independent below about $200K$. Fig. 7.4

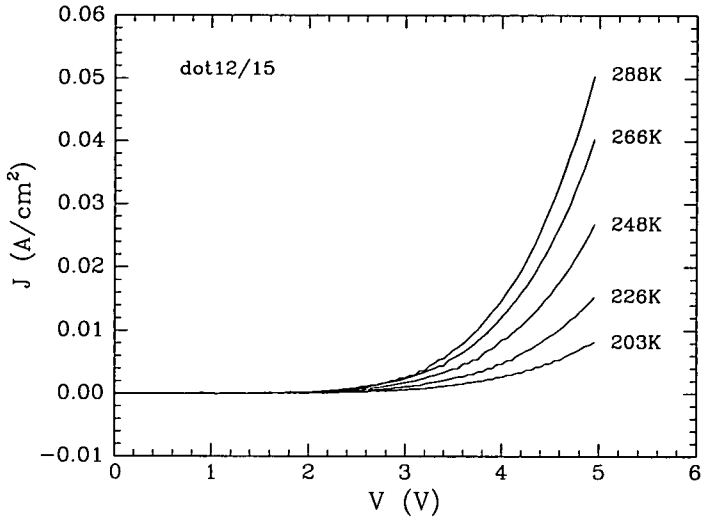


Figure 7.2: J-V characteristics changing with temperature. (samples from batch 96-9, see Table 6.1).

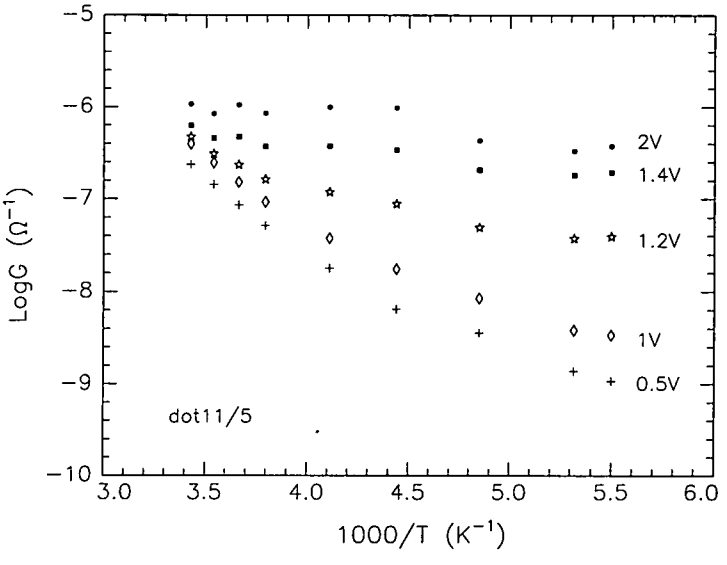


Figure 7.3: Arrhenius plot of the conductance against inverse temperature, with changing voltage biases. (sample from batch New-4, see Table 6.1)

shows the dependence of both E_a and the logarithm of the pre-exponential constant G_0 on reverse bias over the voltage range $0-2V$ and in the temperature region $> 220K$. The changes in both E_a and G_0 with voltage exhibit the characteristics associated with thermionic-field emission (compare with Fig.3.5). At low biases, E_a initially increases and reaches a maximum ($\sim 0.31eV$) at about $0.2V$, then decreases with bias. The prefactor G_0 exhibits a similar

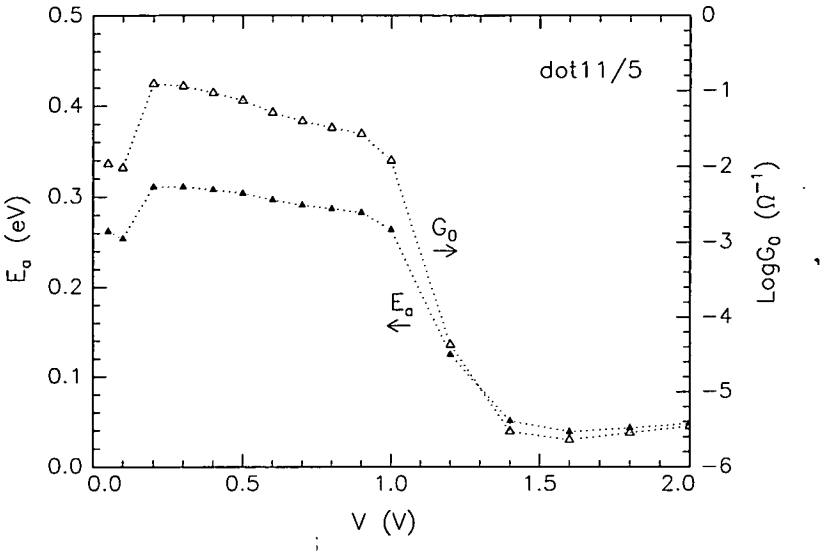


Figure 7.4: E_a and $LogG_0$ *vs.* V.

dependence on voltage and the initial increase in G_0 at low bias may result from the diffusion current, which is proportional to $(\mu\mathcal{E})$ [59, 60]. The subsequent reduction in E_a can be divided two stages: E_a first decreases slowly with voltage when $V <\sim 1V$. At about $1V$, it decreases rapidly to a very low value of $\sim 0.04eV$. Correspondingly, G_0 also decreases rapidly, indicating that tunnelling has set in, which effectively reduces the barrier height of the contact and hence causes a large increase in reverse current. It should be pointed out that the changes in both E_a and G_0 shown in Fig.7.4 reflect general characteristics. There are slight variations among devices, probably due to differences in deposition process. Over many samples E_a is typically in the range $0.15-0.25eV$ at $\sim 0V$, $0.2-0.35eV$ at intermediate biases and $< 0.05eV$ at higher biases (eg $> 1.5V$).

The logarithm of the conductance pre-factor ($LogG_0$) is plotted against E_a in Fig. 7.5, illustrating the correlation between E_a and G_0, i.e:

$$lnG_0 = lnG_{00} + E_a/k_BT_m \tag{7.2}$$

where G_{00} is a constant, and T_m is a "characteristic temperature". Both G_{00} and k_BT_m assume fixed values for related process. This relationship, also

known as the Meyer-Neldel rule [115], has been observed in various inorganic and organic semiconductors and also in undoped and doped a-Si:H [116]. Fitting the data to Eq.(7.2) gives $k_B T_m = 19 - 26meV$, or $T_m = 220 - 300K$,

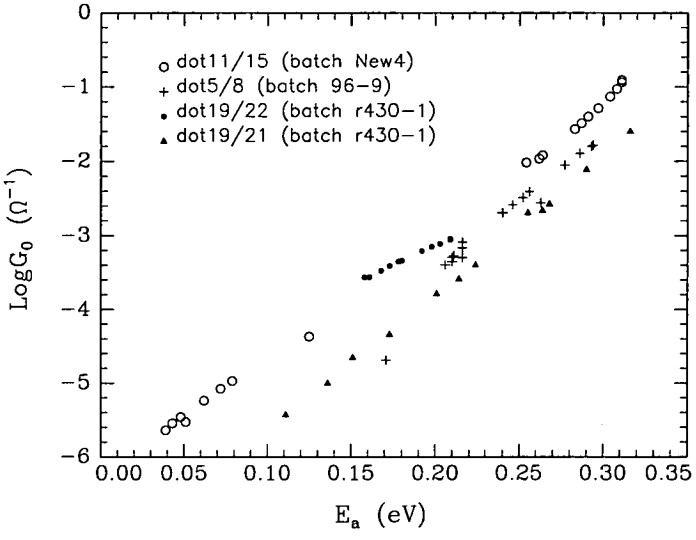


Figure 7.5: $LogG_0$ *vs.* E_a.

which are closed to reported values [117]; G_{00} is in the range $3 \times 10^{-8} - 4 \times 10^{-7}\Omega^{-1}$ for different samples. The underlying mechanisms for a correlation between E_a and G_0 are many fold: eg. intrinsic bulk thermal generation and transport by hopping over an intermolecular barrier, or carrier tunnelling through the barrier, etc. [118]. In the present case hole injection (via tunnelling) from an electrode into the valence band in a reverse biased V/a-Si:H barrier is the most likely reason, consistent with the thermionic-field emission mechanism observed in the J-V characteristics and the bias dependence of E_a.

7.1.3 AC characteristics.

Impedance spectra were measured over the frequency range $1Hz$ to $32MHz$, using a Schlumberger 1260 Impedance/Gain-phase Analyser as described in §6.2. Fig. 7.6 shows a typical plot of the imaginary, $Im(Z)$, versus the real part of the impedance, $Re(Z)$, at different reverse biases: -1.5, -2.1, -2.7

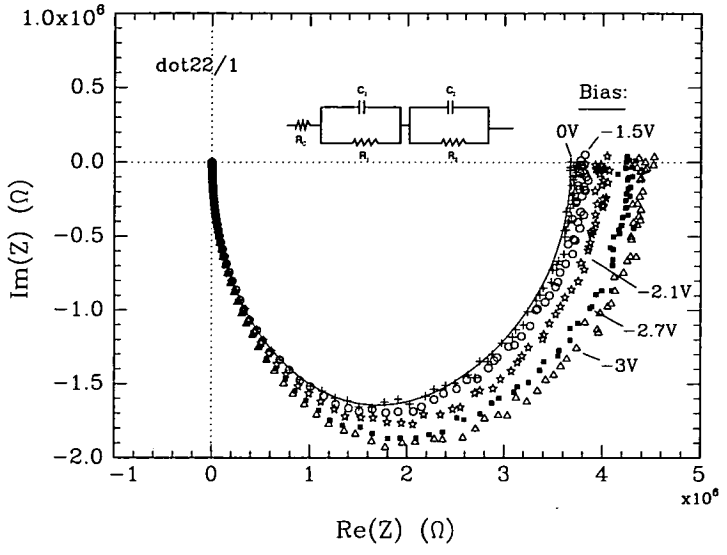


Figure 7.6: $Im(Z)$ *vs.* $Re(Z)$ for an unstressed sample, with an increasing dc reverse bias from $0V$ (un-biased) to $-3V$. The solid line is for the equivalent circuit illustrated in the inserted figure at zero bias, with $C_1 = 853.1pF$, $C_2 = 82.9pF$, $R_1 = 915k\Omega$, $R_2 = 2.76M\Omega$, and $R_C = 77.3\Omega$ (sample from batch R430-4, see Table.6.1).

and $-3V$. The main features can be fitted well using an equivalent circuit consisting of two series-connected parallel RC branches with a contact resistance R_C, as shown in the inserted figure. With increasing the bias from $0V$ to $-3V$, R_1 and C_1 change notably, eg. R_1 increases from $821k\Omega$ to $1.13M\Omega$, while C_1 exhibits a complicated change, first increasing from $851.3pF$ at $0V$ to $931pF$ $(-0.9V)$, then dropping to $800.3pF$ $(-1.2V)$. It increases again with the bias to $880pF$ at $-3V$. On the other hand, R_2, C_2 and the contact resistance R_C are almost constant. The parameters R_1 and C_1 may reflect the barrier properties, while the other branch R_2C_2 represents the bulk. The contact resistance R_C in the example of Fig.7.6 is 77.3Ω, but it varies from several tens to several hundreds of Ohms, depending on the sample, possibly due to variations in the deposition process and connecting leads.

The frequency dependence of the effective capacitance $C(\omega)$ and conductance $G(\omega)$ is obtained by translating the impedance data into admittance using the following equations,

$$Y = \frac{1}{Z} = G(\omega) + j\omega C(\omega) \tag{7.3}$$

with

$$G(\omega) = \frac{Re(Z)}{Re(Z)^2 + Im(Z)^2} \; and \; C(\omega) = \frac{1}{\omega} \frac{-Im(Z)}{Re(Z)^2 + Im(Z)^2} \tag{7.4}$$

where $\omega = 2\pi f$. The capacitance and conductance are both plotted in Fig. 7.7. The capacitance $C(\omega)$ decreases continuously with increasing frequency,

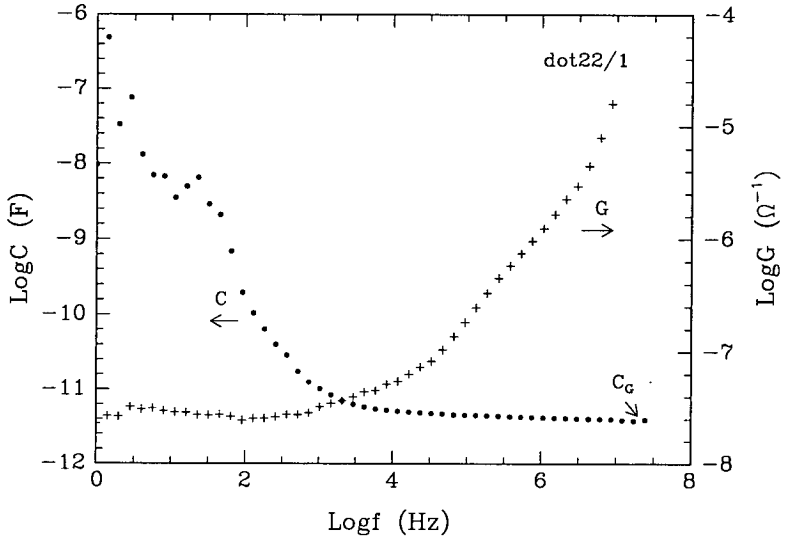


Figure 7.7: $C(\omega)$ & $G(\omega)$ *vs.* frequency (sample from batch R430-4).

dropping rapidly between 10^2 to $10^4\,Hz$, eventually falling to C_G, the geometrical capacitance of the specimen. On the other hand, $G(\omega)$ increases rapidly in the region of $10^4 - 10^5\,Hz$, and it does not saturate at high frequencies. This is due to the effect of the contact resistance, R_C.

Similar features have been observed in other a-Si:H Schottky barriers [6], and were interpreted in terms of an electronic model which combines the density-of-states distribution in a-Si:H, the equivalent circuit of two RC branches in series, and thermionic-field current through the barrier. This mechanism is likely to be applicable in the present case of Cr-p^+a-Si:H-V devices, since the same current transport mechanism and ac characteristic are also observed.

In summary, the current transport in unstressed reverse-biased Cr/p^+a-Si:H/V devices is characterised by thermionic-field emission of carriers through the metal-a-Si:H barrier. The thermal activation energy of conductance is considerably reduced at high fields. Further analysis and discussion is given in the next section.

7.2 Discussion.

It was argued in §7.1 that with increasing voltage, current transport through a reverse-biased V/a-Si:H (or Cr/a-Si:H) barrier exhibits the characteristics associated with quantum mechanic tunnelling. This is consistent with the thermionic-field emission model presented by Padovani *et al* [64] and discussed in §3.2. According to Eq.(3.3), the reverse biased current-voltage characteristic with a tunnelling contribution in moderate voltage region is given by:

$$J = J_s exp(V/E') \ or \ J = J_s exp(-q\phi_{eff}/k_B T) \cdot \tag{7.5}$$

where J_s is the reverse saturation current, ϕ_{eff} is the effective barrier height, and E' is a complicated function of the term E_{00} [Eq.(3.4)], which is related to the N_a (acceptor density), m^* (effective mass), and ϵ_s (relative dielectric constant) according to Eq.(3.5). The parameter $(qE_{00}/k_B T)$ is a measure of the relative importance of tunnelling, as E_{00} is the barrier height where the tunnelling probability is e^{-1} for carriers at the band edge. For crystalline silicon the charge density is simply equal to the dopant density since nearly all dopants are fourfold coordinated and hence electrically active. In the case of a-Si:H, however, the donor (or acceptor) density is not equal to the gas-phase dopant density because the dopants may be in threefold coordinated which will be neutral, and not contribute to the space-charge layer. According to the auto-compensation model [32, 42], doping in a-Si:H will lead to the formation of a large number of charged defects near the quasi-Fermi level. The density of these charged defects is almost equal to that of electrically active fourfold dopants. The acceptor density can be determined therefore from the

charged defect density, which is related to the gas-doping ratio by Eq.(2.5). For B_2H_6/SiH_4 gas-doping ratios of 10^3 to $10^4 ppm$ the defect density (thus N_a) is calculated to be in the range of 3×10^{17} to $\sim 2 \times 10^{18} cm^{-3}$. By treating the effective mass m^* as an adjustable parameter, (qE_{00}/k_BT) is estimated as to be $0.4 - 0.9$ at room temperature for $\epsilon_s = 11.7$, $N_a = 2 \times 10^{18} cm^{-3}$, and $m^* = 0.1 - 0.5 m_0$. Thus (qE_{00}/k_BT) is not too far from unity. Thermionic-field emission is expected therefore to dominate for these doping densities.

Fitting the J-V curves to Eq.(7.5) gives good agreement with experimental results. Fig. 7.8 shows a typical result in which N_a, ϵ_s and m^* are $1.2 \times 10^{18} cm^{-3}$, 11.7, and $0.46 m_0$ respectively. The activation energy ($\sim 0.18 eV$) is

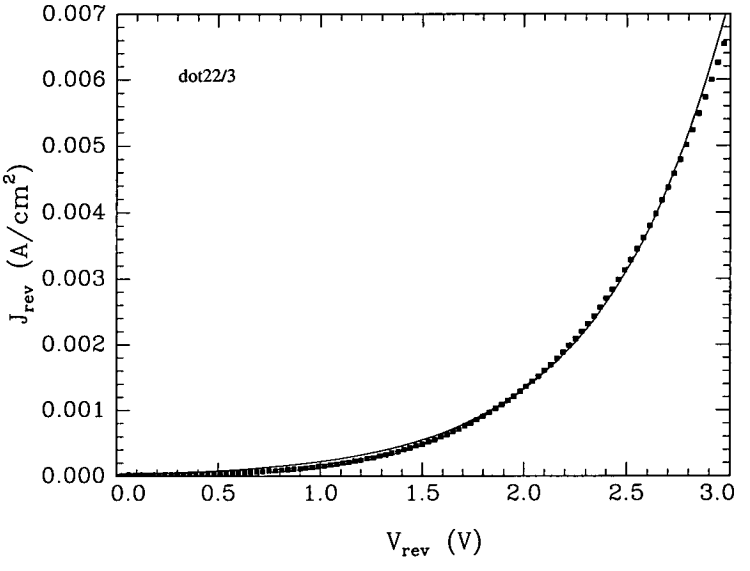


Figure 7.8: A typical fitting result of the J-V characteristic using Eq.(7.5) (sample from batch R430-4).

determined by the doping experiments [111]. The curve fitting gives 0.687 eV for ϕ_{eff}. For different samples ϕ_{eff} is found to vary from 0.55 eV to 0.80 eV, while keeping most of other parameters constant (both E_a and N_a are subjected to the doping level). However, it should be noticed that although ϕ_{eff} is reasonably close to the reported values of $0.64 - 0.65 eV$ for a V/n-type Si Schottky barrier [119,120], and also to many other metal/p-type a-Si:H barriers [121], there is an uncertainty about the exact value of ϕ_{eff} due to the lack of

precise measurements. Moreover, the value for effective mass ($0.46m_0$), while not unreasonable [122], appears arbitrary. The actual ϕ_{eff} may be significantly lower than the above values, if judged from the very low activation energy ($< 0.1eV$, see Fig.7.4) at voltages greater than $1V$.

The tunnelling effect occurring through a reverse-biased V/a-Si:H junction may result from high boron doping in the a-Si:H bulk film. This is very similar to the case of phosphorus-doped a-Si:H barriers [68], where it has been found that ϕ_{eff} exhibits a strong dependence on doping once the doping level is over

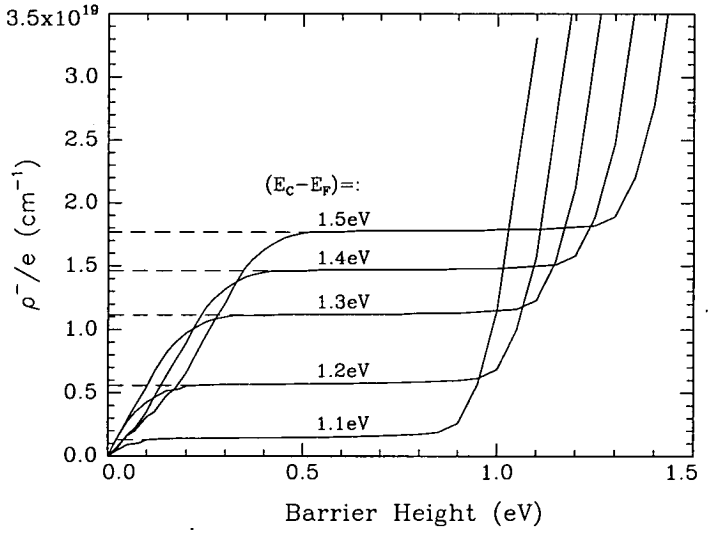


Figure 7.9: Net space charge density (ρ^-/e) as a function of the barrier height for p-type a-Si:H, with the position of Fermi level ranging from $1.1-1.5eV$. The calculation is based on the density-of-states model of Spear *et al* [19].

10 *vppm*. It reduces significantly, even at zero field, with sufficiently high doping densities. Tunnelling is exponentially dependent on the barrier width and it is dramatically enhanced in highly doped specimens. Fig. 7.9 shows calculations of the net space charge density (ρ^-/e) against the barrier height for a series of different Fermi levels position (determined by doping concentration) in metal/p^+a-Si:H barriers.

The barrier profile for p-type metal/a-Si:H junctions is calculated based on the above curves, with the results shown in Fig. 7.10. With increasing doping

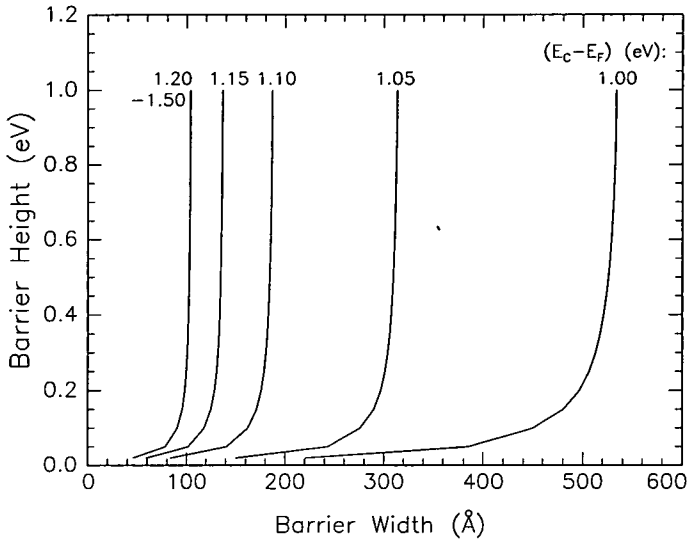


Figure 7.10: Barrier profile for p-type specimens, with the position of Fermi level ranging from $1.0 - 1.5\ eV$. The calculation is based on the density-of-states model of Spear *et al* [19].

concentration the barrier width decreases significantly. In addition, the barrier height *vs.* barrier width curves become increasingly steep. Further increase in doping concentration corresponding to the Fermi level at $\sim 1.2eV$ does not reduce the barrier width due to the non-degenerate character of a-Si:H. Assuming that $E_g = 1.7\,eV$, then for a p-type specimen with activation energy $\sim 0.2\ eV$ (corresponding to a doping ratio of about $10^4\ vppm$), $(E_C - E_F) = 1.50eV$. Therefore, the barrier width estimated from the profile is in a range of $90 - 100$ Å, for a barrier heights ranging from $0.1 - 1eV$.

With an increase in reverse voltage, field-assisted tunnelling is enhanced and hence the effective barrier height ϕ_{eff} further decreases, as predicted by the thermionic-field emission theory. This is reflected in the rapid reduction in activation energy E_a as shown in Fig.7.4 and the exponential increase in current in Fig.7.1. The dominant current path is no longer over the top of the barrier but moves to a lower energy. At high fields where $\mathcal{E} > 2 \times 10^5 V/cm$, it is appropriate to use an effective tunnelling parameter, α, to describe the tunnelling event according to Shannon's model (refer to §3.2). The effective tunnelling parameter, α, extrapolated from measured J-V curves is found to

be in the range $40 - 70\mathring{A}$ in the temperature range $280 - 400K$. The results are plotted in Fig. 7.11, where it is seen that α is almost independent of temperature. A similar result has been reported by Nieuwesteeg *et al* [5].

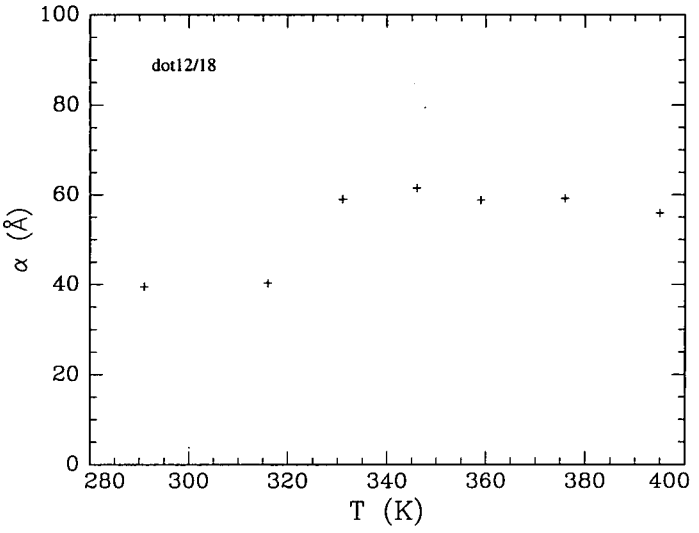


Figure 7.11: Temperature dependence of α as obtained from J-V curves in a high electric field region between $2 \times 10^5 - 7.3 \times 10^5 V/cm$ (sample from Batch96-9).

Chapter 8

Current Stressing and Forming.

8.1 Current stressing.

8.1.1 Variation of voltage with time.

The experimental setup is described in *Chapter* 6, where a HP4145A Semiconductor Parameter Analyser is used to provide voltage/current output for stressing and forming. In the time domain mode, the instrument acts as a current source which stimulates the device, while a voltage monitor records and displays the change in voltage (denoted as V_{mea}) necessary to maintain a constant current with time. During measurements, the positive voltage is

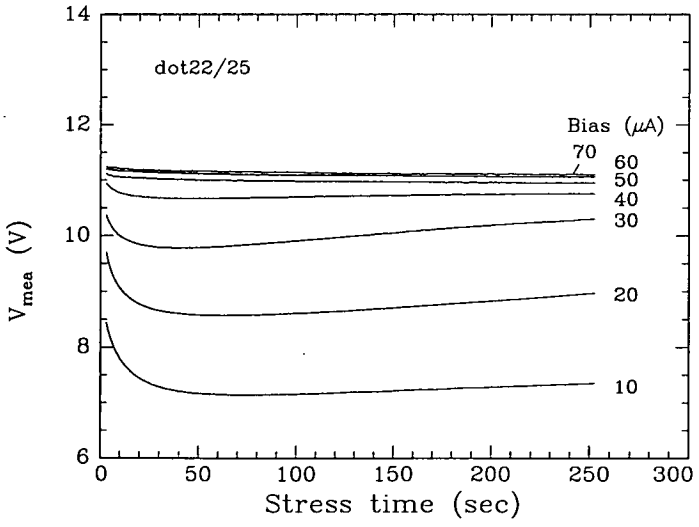


Figure 8.1: Sample voltage (V_{mea}) vs. stressing time for different current biases (samples from batch 10040/13BT, see Table.6.1).

usually applied to the top (vanadium) electrode, so that the V/a-Si:H contact is reverse biased. Fig. 8.1 shows a typical V_{mea} as a function of stress time over a range of constant current bias ($10 - 70\mu A$), with the measurements performed at ambient temperature. For the first several tens of seconds, at the lower current biases, V_{mea} decreases exponentially with time. After that initial decay V_{mea} begins to increase with stressing time and at sufficiently long times it tends to saturate. With increasing current bias the minimum in the V_{mea}-t curves disappears altogether. Eventually, after a sufficient stressing time at a large current bias (e.g.$\sim 74\mu A$, but not shown in Fig.8.1), V_{mea} and the sample resistance drop discontinuously to a low value. The device is then in the electroformed state, and the forming process itself is described in § 8.2. The overall features of $V_{mea}(t)$ shown in Fig.8.1 can be fitted to the following empirical formulae,

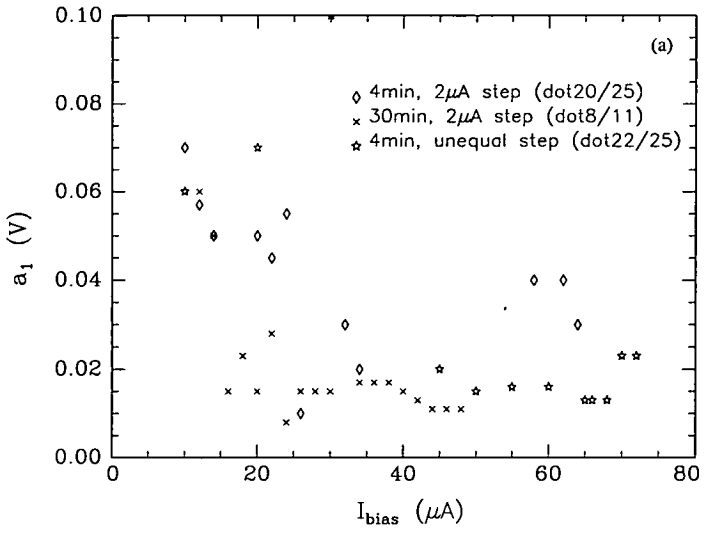
$$V_{mea}(t) = a_1 exp[-a_2(t - t_0)] \quad (initially) \tag{8.1}$$

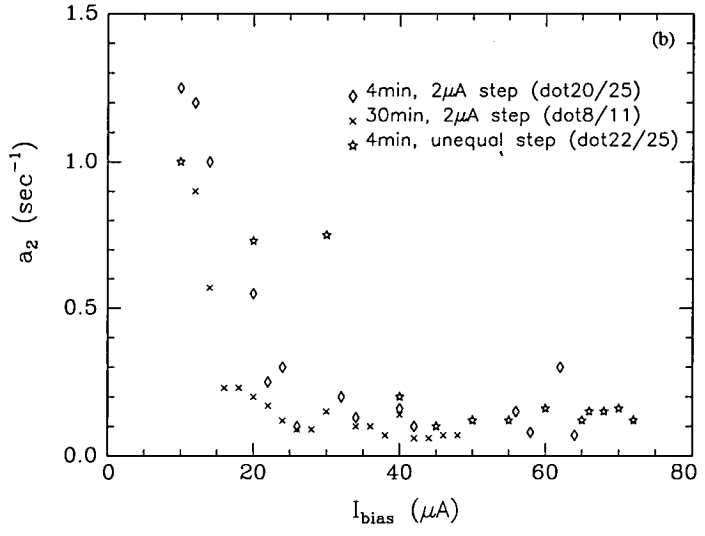
and subsequently

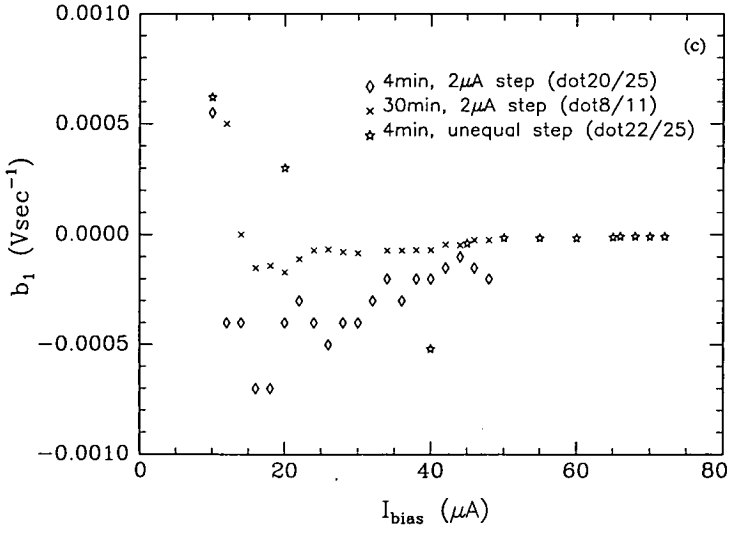
$$V_{mea}(t) = V_0 + b_1 t + b_2 t^2 \tag{8.2}$$

where t_0 is determined by the delay time of the HP4145A Analyser, and a_1 & a_2, b_1 & b_2, and V_0 all describe features of $V_{mea}(t)$. They are usually both bias and stress time-dependent.

Figs. 8.2(a) to (e) show the current bias (I_{bias}) dependence of these parameters. In the experiments, the current bias is applied to the specimen under test with increasing magnitude from $1\mu A$ to $72\mu A$. The increment in bias was either kept constant (i.e.$2\mu A$), predetermined by the programming, or chosen manually in unequal steps. In each period of stressing, the stress time was altered (i.e.$4 min$ or 30 min) for different samples. In this way, stressing effects under various conditions can be compared. Several features should be noted in these results.


(a)
◊ 4min, 2μA step (dot20/25)
× 30min, 2μA step (dot8/11)
☆ 4min, unequal step (dot22/25)
a1 (V)
0.10
0.08
0.06
0.04
0.02
0.00
0
20
40
60
80
Ibias (μA)


(b)
◊ 4min, 2μA step (dot20/25)
× 30min, 2μA step (dot8/11)
☆ 4min, unequal step (dot22/25)
a2 (sec−1)
1.5
1.0
0.5
0.0
0
20
40
60
80
Ibias (μA)


(c)
◊ 4min, 2μA step (dot20/25)
× 30min, 2μA step (dot8/11)
☆ 4min, unequal step (dot22/25)
b1 (Vsec−1)
0.0010
0.0005
0.0000
−0.0005
−0.0010
0
20
40
60
80
Ibias (μA)

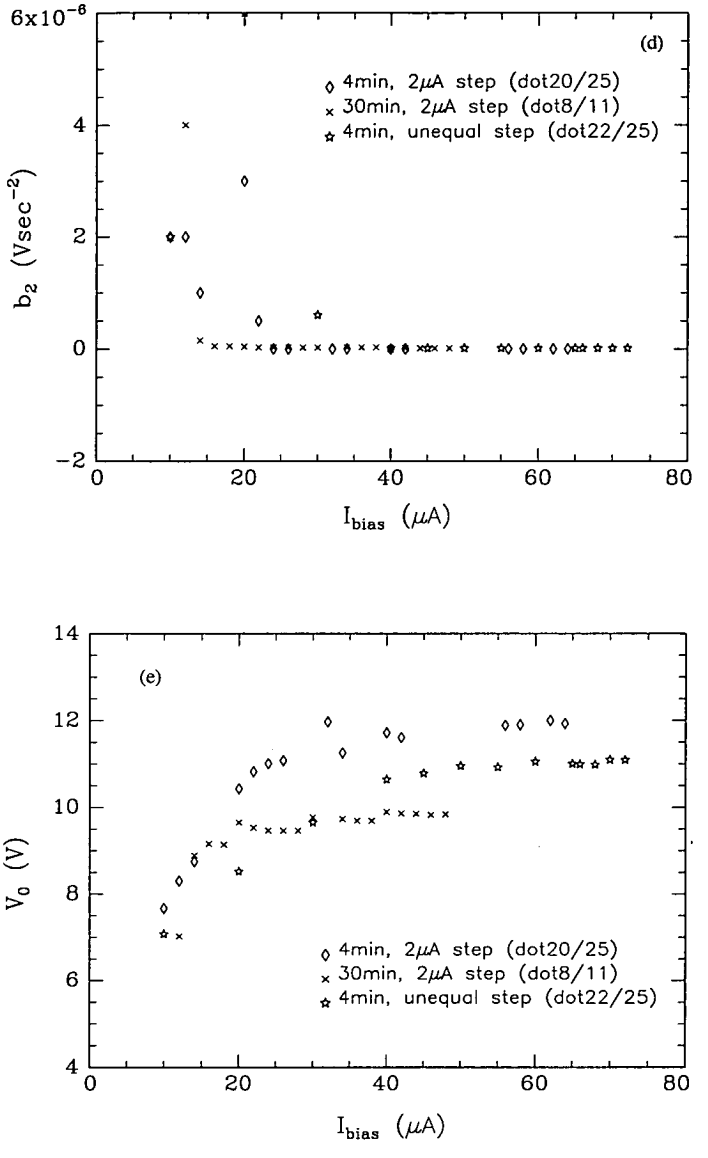


Figure 8.2: a_1, a_2, b_1, b_2 and V_0 *vs.* I_{bias} (sample from batch 10040/13BT).

Firstly, there are systematic changes in each of the parameters with current bias, regardless of variations in stress conditions. Secondly, a_1 & a_2, and b_1 & b_2 become very small, or nearly zero, at a sufficiently large I_{bias} where V_{mea} becomes linear. Thirdly, V_0, which reflects the magnitude of $V_{mea}(t)$, increases rapidly from a lower value of $6-7V$ to about $10V$ when I_{bias} reaches $30-40\mu A$, and it then increases gradually to a saturation value. Although the saturated value varies for different stressing conditions, the initial change in the range of $10-30\mu A$ is almost identical.

At a fixed constant current bias, prolonging the stress time causes a very similar change in the $V_{mea}(t)$ *vs.* t characteristics. This is shown in Fig. 8.3 and Fig. 8.4, which show the typical time dependence of b_1, b_2 and V_0 respectively, for a sample stressed at $5\mu A$ at room temperature. The similar effects caused by

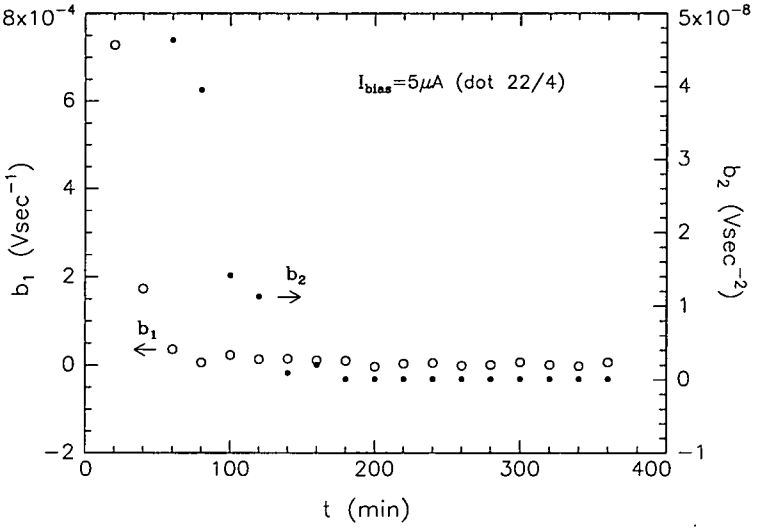


Figure 8.3: b_1 and b_2 *vs.* t (sample from batch 10040/13BT-2).

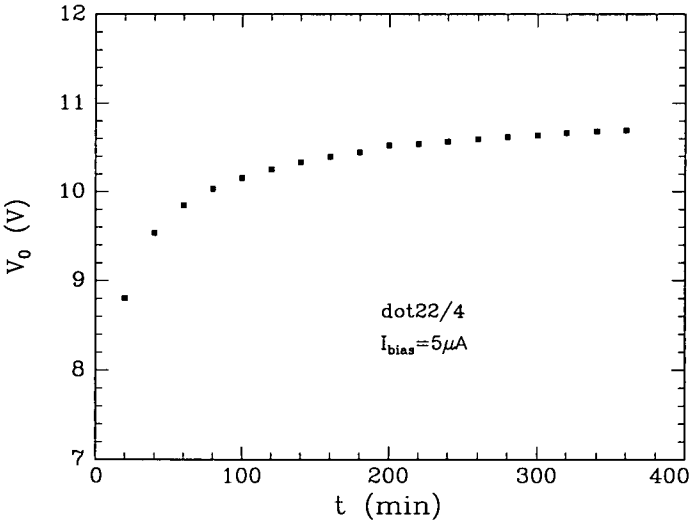


Figure 8.4: V_0 *vs.* t (sample from batch 10040/13BT-2).

either constant bias or stressing time suggest that the integrated charge ($= \int I_{bias} dt$), rather than either I_{bias} or stress time alone, plays the important role in the observed V_{mea} *vs* t characteristics. In addition, the change in V_0 (thus

in V_{mea}) indicates that the injection of carriers from the electrodes causes defect creation and/or charge trapping within the device under stress. New defects and/or trapping causes a reduction in the current through the device and V_{mea} increases to maintain the constant current. This is also evident in the observation of a decrease in reverse current (or current density) with both increasing current bias and stress time (see next section).

As discussed later in §8.4, the initial reduction in V_{mea} (see Fig.8.1) might result from a mechanism associated with electron trapping rather than hole trapping caused by a long-time or high current-bias stress. This leads to a temporal reduction in device resistance and thus V_{mea}. Noted that a similar initial anomalous change has been also observed in thin oxide films under a constant voltage stress [123].

8.1.2 Changes in J-V characteristics during current stressing.

Fig. 8.5 illustrates typical changes in device I-V characteristic during the course of current stressing. The solid and dashed lines are I-V curves before and after stressing respectively. For convenience, the negative quadrant has been turned

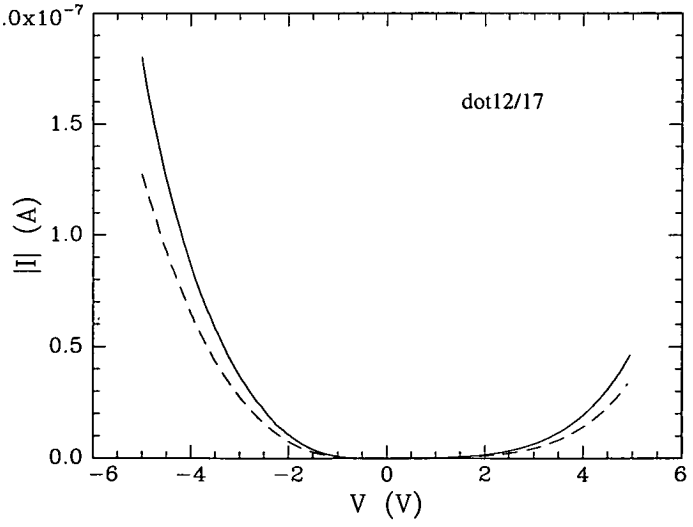


Figure 8.5: Shift in I-V characteristic after stressing at 1 nA for 100 min at ambient temperature (sample from batch 96-9).

through 180°. In some cases, i.e. at very low current bias or short stress time, anomalous *increases* in current were also observed. The general trend, however, is for the current at a given voltage, in either the forward or reverse direction, to decrease with either a prolonged stress time or increasing current biases during current stressing.

Typical changes in the J-V characteristics during prolonged current stressing are shown in Fig. 8.6. In the experiment from which Fig.8.6 was constructed,

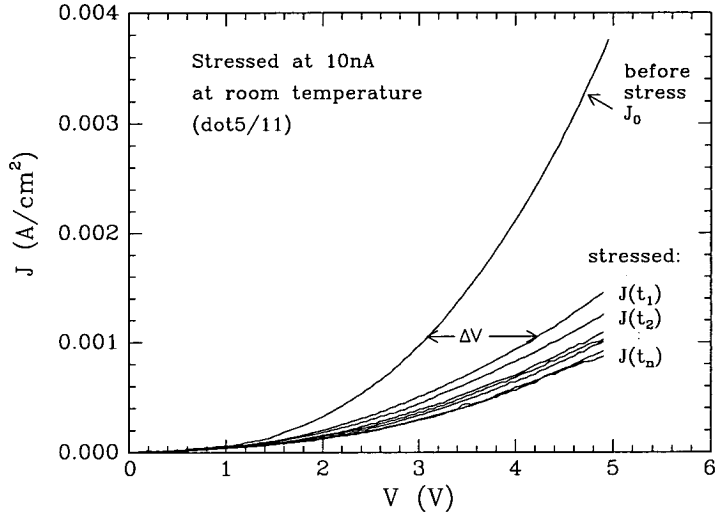


Figure 8.6: J *vs.* V characteristic stressed under a $10nA$ current bias for different stressing times, with $t_1 = 30min$, $t_2 = 2t_1$, ..., $t_n = nt_1$ (sample from batch 96-9).

the current stress was interrupted briefly at predetermined intervals (i.e.$30min$ in this case), and the J-V characteristic of the device under stressing was measured immediately. Care was taken not to influence the electrical properties of the device during measurement. Under a $10\,nA$ constant current stress J decreases but there is large drop in J in the first period (indicated by $J(t_1)$), and a lesser reduction at later stages (indicated by $J(t_2)$, $J(t_3)$,..., $J(t_n)$, respectively). This change in J can be described in terms of the voltage shift ΔV, defined as the difference between voltages measured at different times ($V(t_i)$) and the initial voltage ($V(0)$) at the same reverse current density, as illustrated in Fig. 8.6. If there is no change, $\Delta V = 0$; $\Delta V > 0$ or < 0 corresponding,

respectively, to a decrease or increase in current due to stressing. The voltage shift ΔV has a specific time and current bias dependence given by:

$$\Delta V = kI^{1/2}t^{\lambda} \tag{8.3}$$

where k, λ are constants. The constant k is dependent on both temperature and the voltage at which J is measured, but λ is found to vary with voltage. There is a reciprocal relationship between stressing current and time .

The stress time dependence of the voltage shift ΔV is shown in Fig. 8.7.

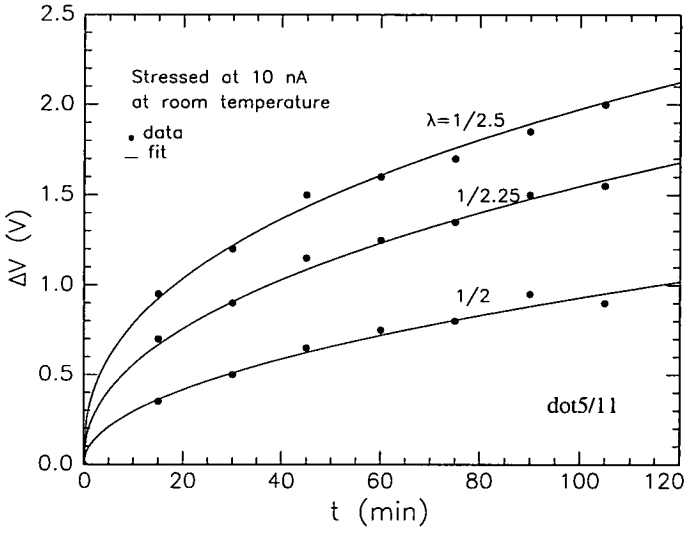


Figure 8.7: Time dependence of ΔV measured at different constant currents. The solid lines are the fitting results using Eq.(8.3) for three sets of data measured at $2.093 \times 10^{-10}A$, $4.958 \times 10^{-10}A$, and $7.428 \times 10^{-10}A$. The fitting index λ for these data is (1/2), (1/2.25), and (1/2.5) respectively (sample from batch 96-9).

These results correspond to the empirical relation Eq.(8.3). The index λ is typically equal to (1/2), and shifts slightly toward a lower value when measured at a higher reverse current.

Fig. 8.8 shows the dependence of ΔV on the bias (I_{bias}), measured at two different temperatures: $337K$ and $290K$. The solid lines are from Eq.(8.3) with k equal to $0.2VA^{-1/2}sec^{-1/2}$ at $337K$ (k_1) and $0.085VA^{-1/2}sec^{-1/2}$ (k_2) at $290K$. Note also that ΔV first decreases, then increases. Similar results

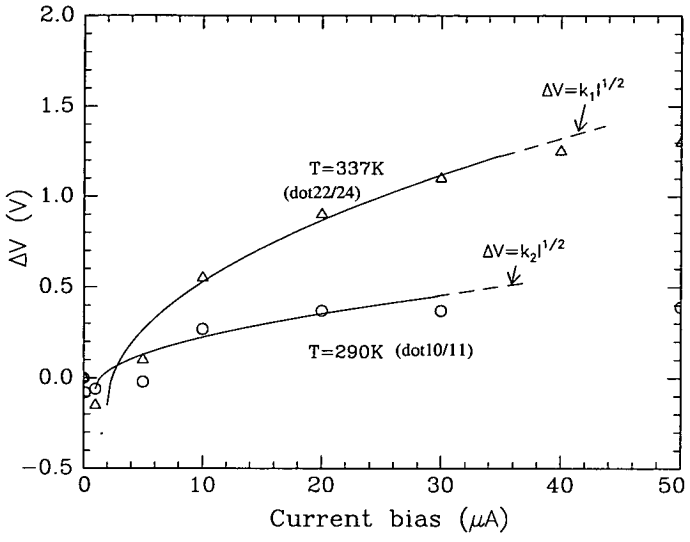


Figure 8.8: ΔV *vs.* current bias, measured at $337K$ (open triangles), $290K$ (open circles) respectively. The solid lines are derived from by Eq.(8.3) with the stress time kept at $30min$ (samples dot22/24 from batch New-6 and dot10/11 from batch r430-5, see Table.6.1).

have been observed in amorphous silicon nitride thin film diodes when stressed under constant current conditions [14].

8.1.3 Temperature effect on the stressing.

Current stressing experiments were also carried out at low temperatures.

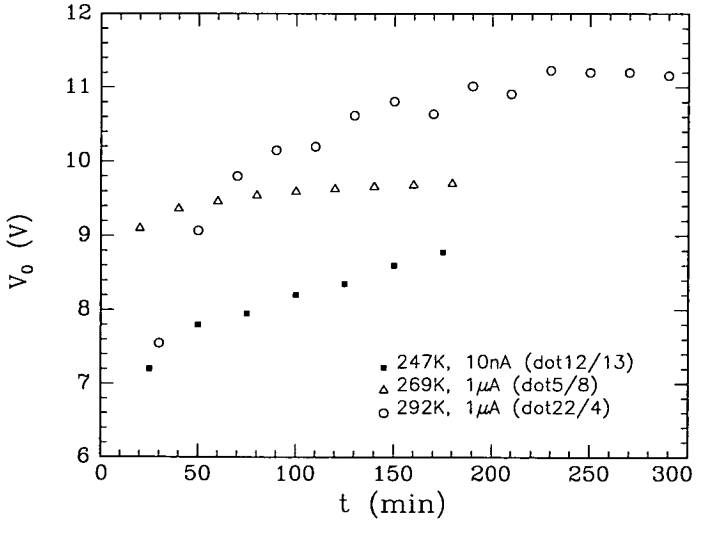


Figure 8.9: V_0 *vs.* t. at $247K$, $269K$ and $292K$ (dot12/13 from batch 96-9, dot5/8 from r430-4, and dot22/4 from 10040/13BT-3).

Fig. 8.9 illustrates changes in V_0 (the magnitude of V_{mea}) with stress time (t) for three samples at $247K$, $269K$ and $292K$. There are slight differences in magnitude of V_0 probably due to differences in sample resistance. However, they exhibit a general trend similar to that shown in Fig.8.2(e). The variation in the constant k in Eq.(8.3) with temperature is shown in Fig. 8.10, in which two sets of data measured at $T = 365\ K$ and $T = 266K$ are presented. In this

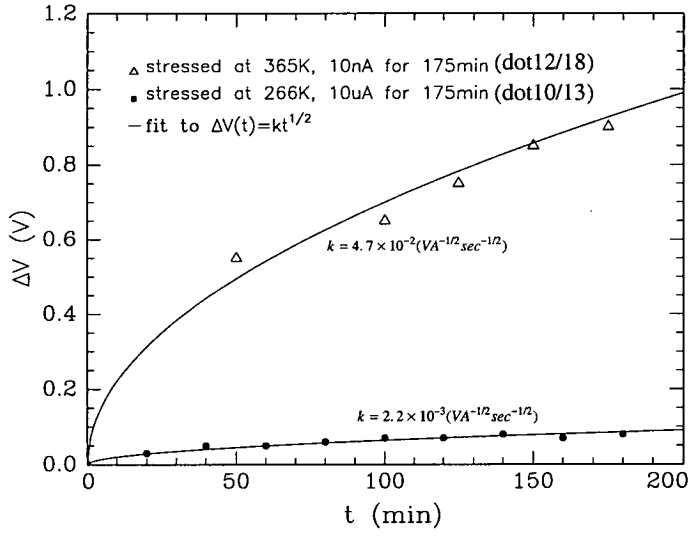


Figure 8.10: Time dependence of ΔV measured at $365K$ (open triangles) and $266K$ (solid squares). The solid lines are fitting results using Eq.(8.3) with $k_{365k} = 4.7 \times 10^{-2} VA^{-1/2} sec^{-1/2}$ and $k_{266k} = 2.2 \times 10^{-3} VA^{-1/2} sec^{-1/2}$ (samples dot12/18 from batch r430-5 and dot10/13 from batch 96-9, see Table.6.1).

temperature range, the relationship between ΔV and stress time can be also fitted well using Eq.(8.3) at a given current density ($\sim 1 mA/cm^2$). The constant k increases with increasing temperature.

It is interesting to note that square-root kinetics are frequently observed in defect generation processes in other a-Si:H diode structures when stressed with a constant current, although the bias dependence of ΔV is different [14, 36]. This suggests that a similar defect creation mechanism may occur in Cr-p^+a-Si:H-V devices during stressing.

8.1.4 Post-stressing changes in device conductance.

Experiments have further shown that even after the cessation of constant current stressing, the conductance of a sample continues to decrease with time. Fig. 8.11 shows results measured at room temperature, but at different voltages (2 to 4.9 V) for the same sample. The parameter G_{t0} denotes the conductance

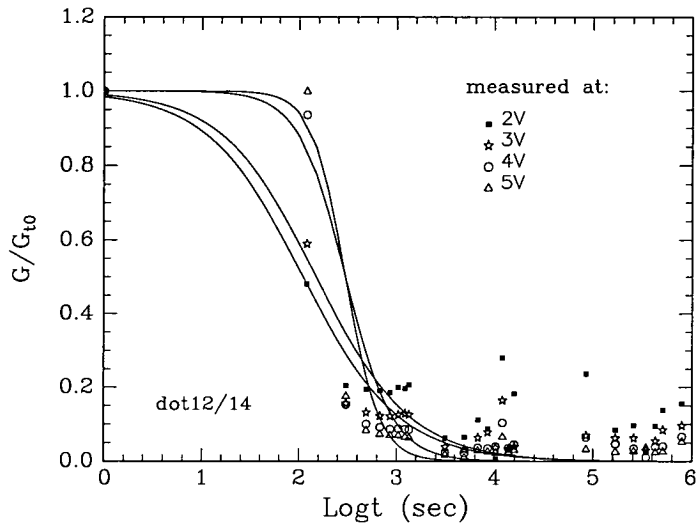


Figure 8.11: G/G_{t0} *vs* t, where data measured at different voltage are represented by solid squares ($2V$), stars ($3V$), open circles ($4V$), and open triangles ($4.9V$) respectively. The solid lines are fitted results using Eq.(8.4) (sample from batch 96-9).

measured at the time when prolonged current stressing ceased, while (G/G_{t0}) is the fractional change measured subsequently. The conductance gradually decays with the time, stabilising at sufficiently long times. The time dependence follows a stretched-exponential relation given by

$$G(t) = G_{t0} exp[-(\frac{t}{\tau})^{\beta}] \tag{8.4}$$

where τ is a time constant, and β is a dispersion parameter, both of which are found to be voltage and temperature dependent. Fitting the data in Fig.8.11 to Eq.(8.4) reveals that on increasing the voltage from $2V$ to $4.9V$, τ increases from $110\,sec$ to $> 300\,sec$, while β increases from 0.4 to 2.5. It is also observed

that τ varies exponentially with reciprocal temperature and from the plot of $Log\tau$ *vs.* $1/T$ in Fig. 8.12, the thermal activation energy is $\sim 1eV$ at $2V$, and $\sim 0.9eV$ at $3V$. It was not possible measure the activation energy at higher voltage. In addition, β changes linearly with temperature, with a slope of

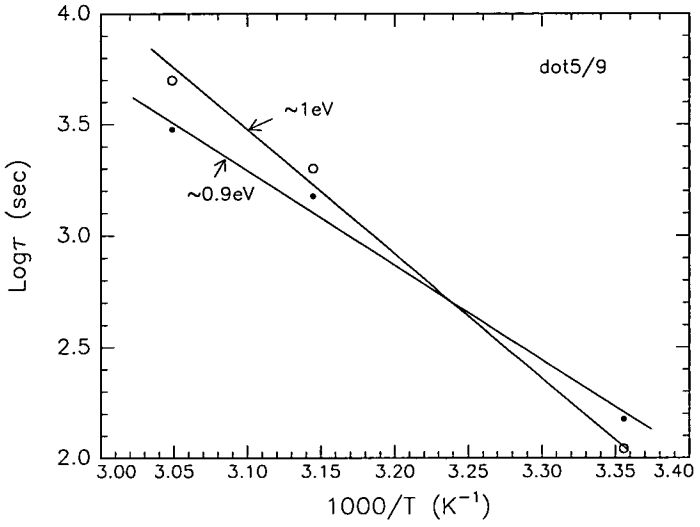


Figure 8.12: $Log\tau$ *vs.* $1/T$, measured at $2V$ (open circles) and $3V$ (solid circles) (sample from batch 96-9).

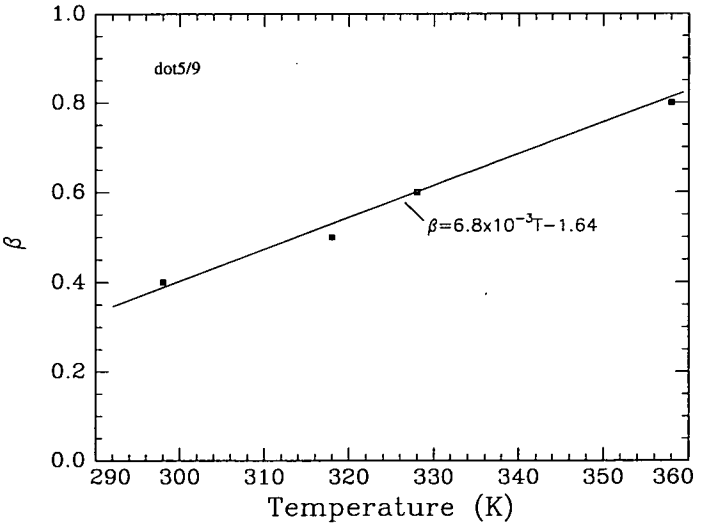


Figure 8.13: β *vs.* T, measured at $2V$ (sample from batch 96-9).

$6.8\times10^{-3}K^{-1}$, as shown in Fig. 8.13. It is interesting to note that the stretched-exponential time dependence characteristic described above is widely observed

in some voltage-stressed a-Si:H devices such as capacitors [56], or in thermally-quenched a-Si:H materials [47].

8.2 Forming.

On progressively increasing the current bias, the device reaches a critical stage at which forming occurs. The overall terminal resistance of device drops from several hundreds megohms to several hundred or several thousand Ohms. Fig. 8.14 shows a typical plot of V_{mea} against the stress time, biased with a range of constant currents from $12\mu A$ to $64\mu A$. At lower bias, the V_{mea} *vs.* t curves

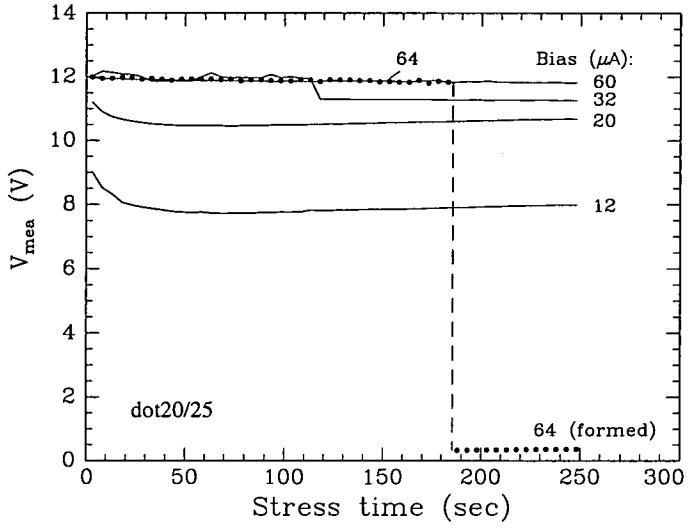


Figure 8.14: V_{mea} *vs.* t under a series of current bias from $12\mu A$ to $64\mu A$ (sample from batch 10040/13BT).

follows Eqs.(8.1) and (8.2). With increasing bias, V_{mea} becomes unstable, and starts to decrease after it reaches saturation at $\sim 60\mu A$. At $64\mu A$, V_{mea} drops rapidly to a very low value ($0.36V$). After the initial increase, the average resistance of the device suddenly reduces to about $3.55k\Omega$, as shown in Fig. 8.15. This corresponds to the low resistance On-state in voltage-formed a-Si:H switching devices. The exact forming current I_F, defined as the bias at which a sample becomes eventually formed, varies from sample to sample. Typically, I_F is tens of micro-amperes. It was found that the history of samples after preparation affects I_F, that is, for freshly prepared specimens, I_F tends to be

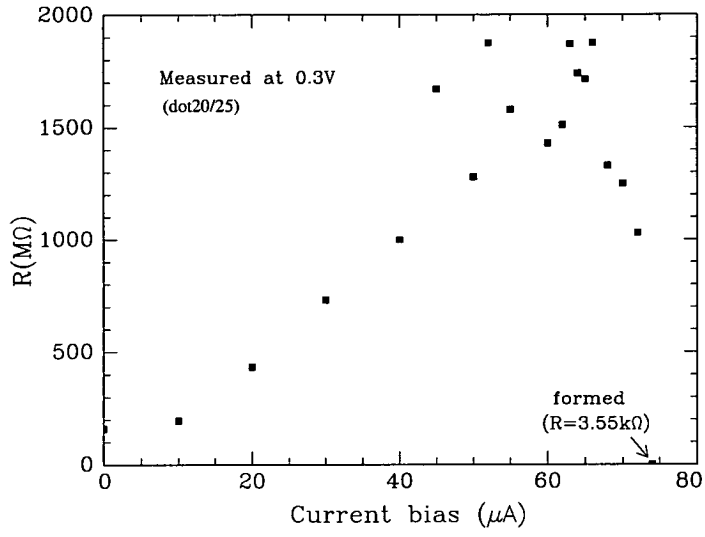


Figure 8.15: Change in device resistance with current bias (sample from batch 10040/13BT).

lower, and vice versa. This may result from oxidation of the top electrode (V) surface. In addition, the bonding process seems to affect I_F as it sometimes varies from chip to chip. In spite of such variation in I_F it is interesting to note that the saturation value of V_0 $(10 - 12V)$ is close to the forming voltage $(12 - 14V)$ seen in the case of voltage-biased forming [10].

Device forming can also be described in terms of the voltage shift ΔV in the

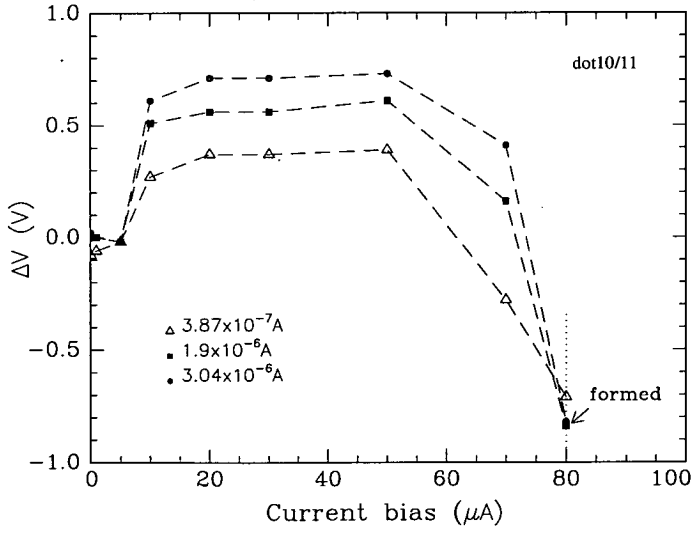


Figure 8.16: Change in ΔV during forming (sample from batch r430-5).

I-V characteristic. A continuous change in ΔV has been found during the progress from the unstressed state to slightly stressed, and the state just before the eventual forming, as shown in Fig. 8.16. At low current bias ($< 15\mu A$), ΔV changes in a manner expressed by Eq.(8.3). At about $20\mu A$, it reaches a saturation. Further increasing the bias to about $50\mu A$ causes a gradual reduction in ΔV. Once ΔV changes its sign from positive to negative at about $70\mu A$, the drop in ΔV accelerates, which means a rapid increase in

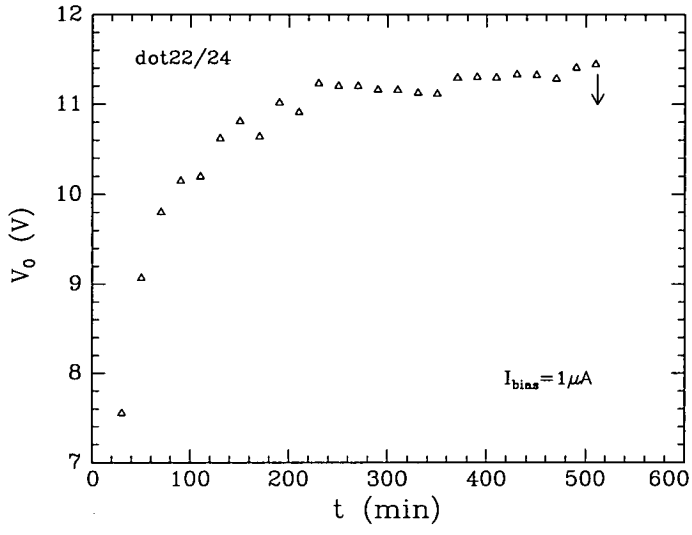


Figure 8.17: V_0 *vs.* t (sample from batch r430-4).

device current. It was also observed that prolonging the stress time at fixed current bias caused forming of the devices. Fig. 8.17 shows this result at room temperature. The voltage V_0 (the magnitude of V_{mea}) increases rapidly with stressing time to almost $10 - 11V$; it then slowly saturates and eventually the devices become formed.

The similarity in the change of V_{mea} with both bias and time suggests that device forming may be related to the total charge injected into the device, i.e:

$$Q_f = \int_0^{t_f} I dt = I t_f \tag{8.5}$$

where I is the bias current, and t_f is the time necessary for forming. Like

I_F, a variation in Q_f exists in different samples. Typically it is in the range $0.011 - 0.032C$.

The experimental results presented above show that current-biased forming is generally characterised by an abrupt change in terminal resistance during the course of forming. This may result from microscopic processes associated with the changes in the microstructure of the specimens under forming, such as avalanche or hot electrons. Further discussions about forming mechanisms are presented in § 8.4.3 of this Chapter.

8.3 Properties of formed devices.

8.3.1 DC characteristics.

After forming, the device resistance drops typically from several hundred megohms to a few kilohms. Fig. 8.18 shows a set of typical I-V characteristics of formed

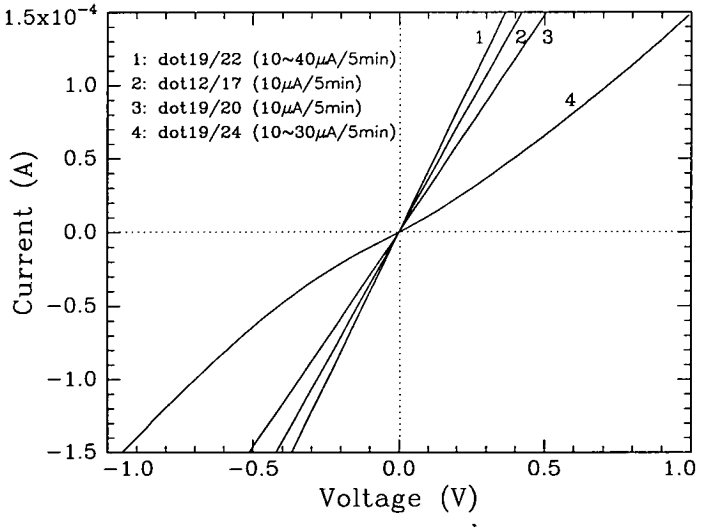


Figure 8.18: I-V characteristic of four formed devices on a same chip. The device resistance, measured at $0.1V$, is 1861, 2240, 2410, and 2770Ω, corresponding to curve 1, 2, 3, and 4 respectively (sample from batch 96-9).

devices. The I-V characteristics usually exhibit a linear relation, as in an Ohmic contact. In higher resistance states, eg.curve 4, a non-linear I-V char-

acteristic develops.

The temperature dependence of these formed states was measured over a range $200 - 300K$, and Fig. 8.19 shows the Arrhenius plot of conductances for two formed devices with different resistances (1134Ω and $26.4k\Omega$). The electro-

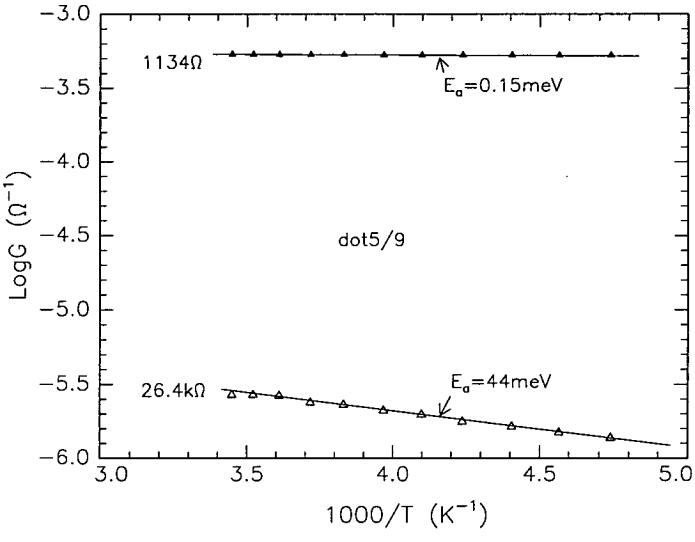


Figure 8.19: Arrhenius plot of dc conductance at two device resistances (sample from batch 96-9).

forming not only causes a substantial decreases in device resistance, but also leads to very low thermal activation energies, from the original $\sim 0.2eV$ to a

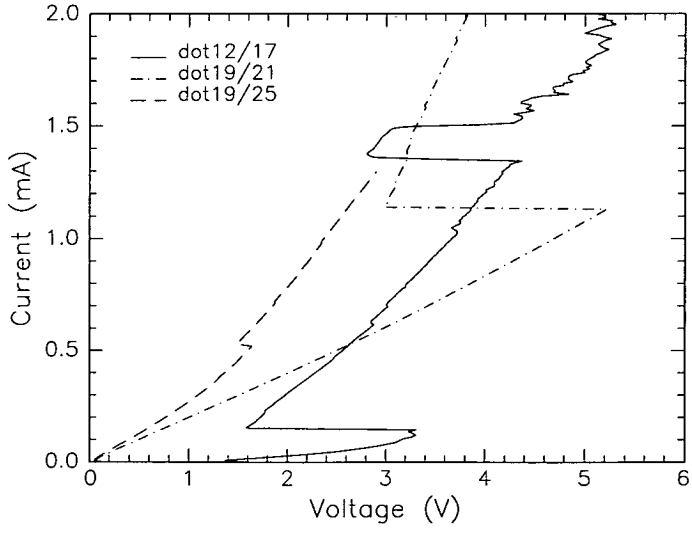


Figure 8.20: I-V characteristics of formed devices under constant current mode (sample from batch 96-9).

a few or few tens of meV, indicating a modification in transport mechanism. It is also found that the I-V characteristics, when measured under constant current conditions, exhibit a negative differential resistance (NDR), as shown in Fig. 8.20. This feature indicates that, like voltage-formed memory devices, filamentary conduction also exists in constant-current-formed devices.

8.3.2 Dynamic switching characteristics.

The switching operation was performed using a HP8110A pulse generator and recorded by a HP54200A digital oscilloscope. The memory resistance is determined at $0.1V$ from the I-V characteristic. Typical waveforms of both voltage and current during both WRITE (OFF to ON) and ERASE (ON to OFF) are shown in Fig. 8.21. Note that the device current responds essentially instantaneously to the voltage signal. There is almost no delay time in the response of the switch, at least as on the time-scale of these measurements.

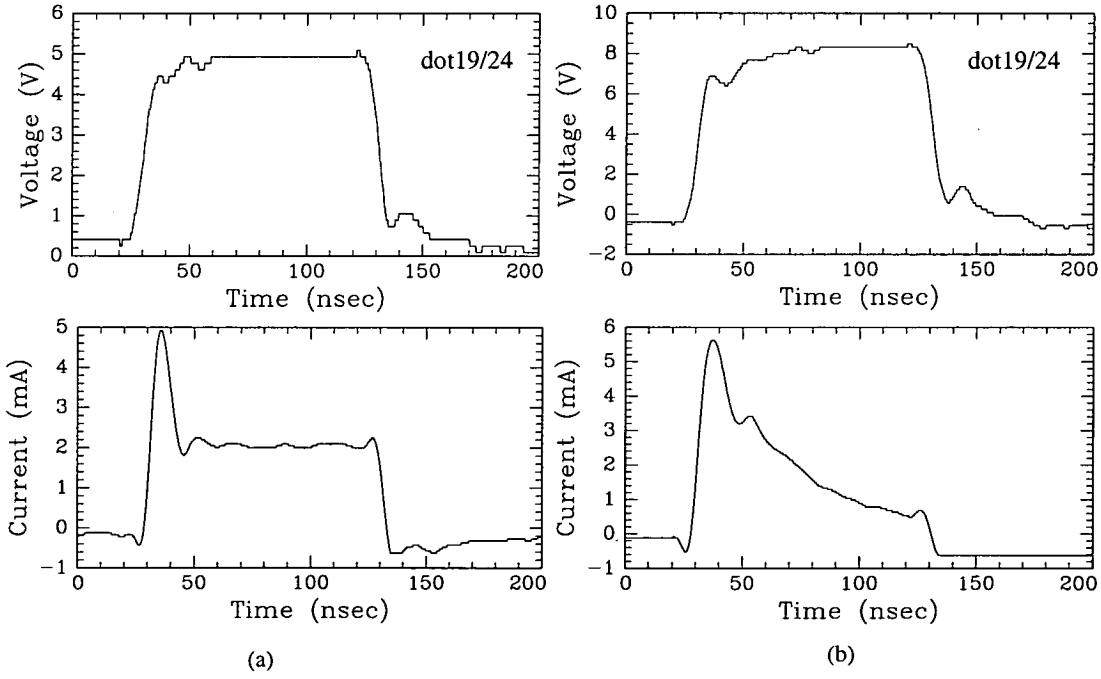


Figure 8.21: Voltage and current waveforms of a single pulse for ON state (a) and OFF state (b) during switching operation (sample from batch 96-9).

In addition, polarity dependence of the switching is usually observed. For example, in the ERASE operation during which the device resistance is switched from low to high, the top electrode must be positively biased with a voltage pulse (pulse width typically in 100 nano seconds); while a negative pulse is required to change the resistance from high to low during the WRITE operation. These are clearly illustrated in Fig. 8.22 and Fig. 8.23 respectively.

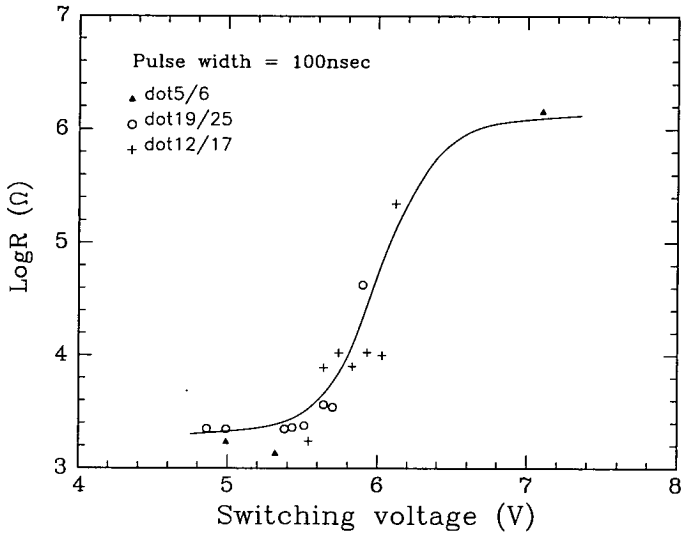


Figure 8.22: Change in device resistance with the switching voltage (pulse amplitude) during the ERASE operation. For clarity a solid line is drawn to guide the eyes (sample from batch 96-9).

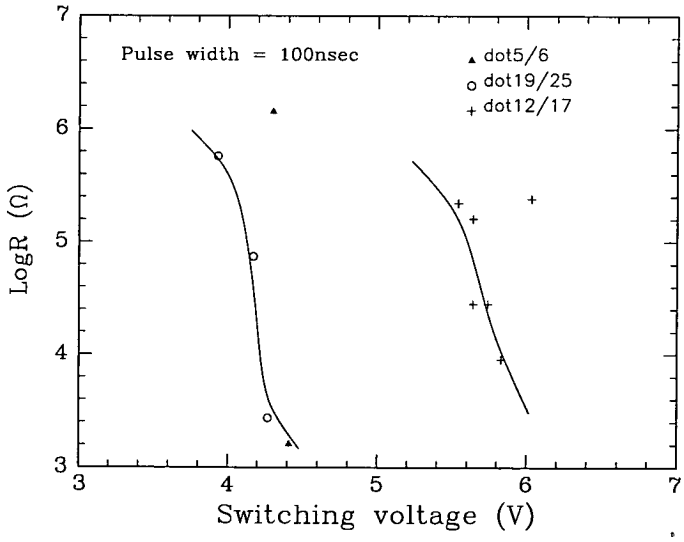


Figure 8.23: Change in device resistance with the switching voltage (pulse amplitude) during the WRITE operation. For clarity solid lines are drawn to guide the eyes (sample from batch 96-9).

With the change of device resistance, the I-V characteristics change from a linear form in the ON-state to a highly non-linear one in (or near) the OFF-state, as shown in Fig. 8.24. This again suggests that a modification in carrier transport occurs during switching.

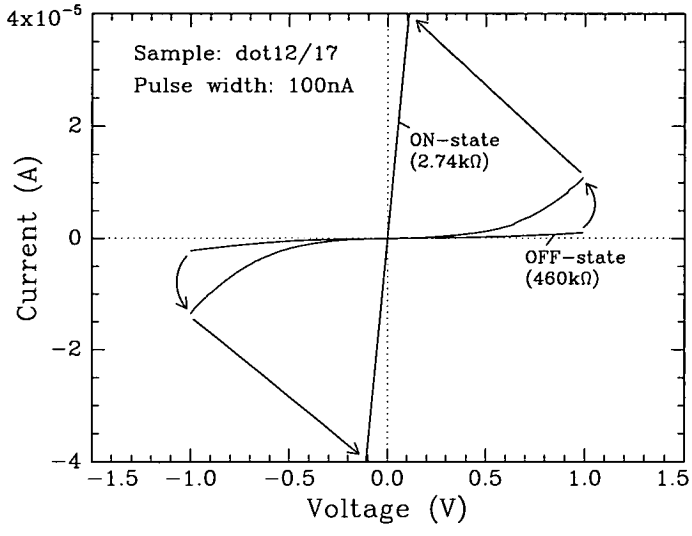


Figure 8.24: Change in I-V characteristic with device resistance (sample from batch 96-9).

Generally, the electrical properties of current-formed devices presented above are very similar to those formed by voltage biasing, probably due to the similar microstructure of the conducting filament after forming. More detailed discussions about the conducting filament will be given in *Chapter* 9.

8.3.3 Metal-non metal transition.

A few constant current formed samples exhibit another characteristic found also in voltage-biased forming. When the temperature is varied, these devices show a metal-non metal (MNM) transition at a low temperature. A typical curve of such a MNM transition is shown in Fig. 8.25, in which, T_{tr} indicates the transition temperature. In the temperature region from $13K$ to about 60K the resistance decreases with increasing temperature, indicating that the conduction process is of a semiconductor type. Between $60 - 100K$ there is a

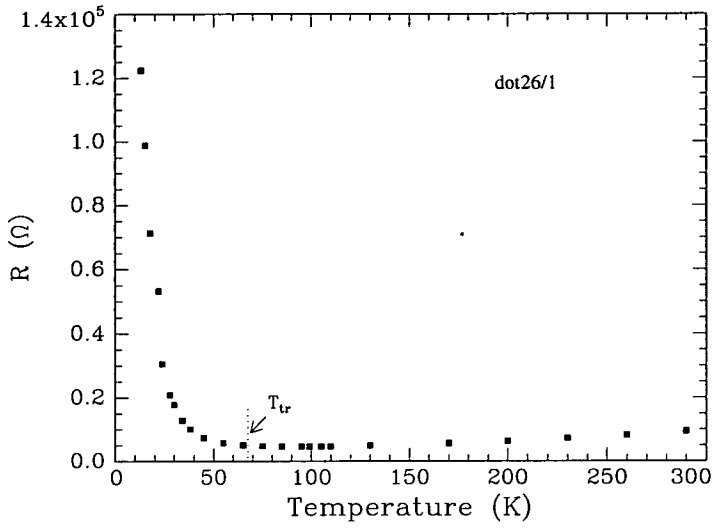


Figure 8.25: DC resistance as a function of temperature (sample from batch 10070/14BT, see Table.6.1).

region where the resistance undergoes a continuous change. It first decreases slightly to a minimum value and then increases almost linearly with increasing temperature indicating a metallic type of conduction. The ac characteristics of these devices also exhibit a notable change near T_{tr} (see §9.1.2). The transition temperature, T_{tr} at which the minimum resistance occurs, is found to be within a range from 60 to $100K$ in different samples. This variation probably results from variations in the forming process, which at the moment cannot be controlled precisely. In *Chapter* 9, more detailed results and analysis of the MNM transition in formed devices will be presented and further discussed.

8.4 Analysis and Discussion.

8.4.1 Defect creation and carrier trapping.

With the injection of charge, via increasing either the current bias or stress time, the device current exhibits an instability, as shown by the shift in I-V (or J-V) characteristics prior to the eventual forming of the device (Fig.8.5 and Fig.8.6). This suggests that defect generation and/or charge trapping might occur during current stressing. Since the current is carried predominantly by holes injected from the reverse biased V-p^+a-Si:H barrier, the reduction in

reverse current suggests that the holes might be responsible for defect creation, i.e. by the occupation of weak Si-Si bond sites in the valence band tail where a high density of defect states exists. As a result of hole trapping, a net positive charge density N_D will develop which leads to a change in the electric field at the V-p^+a-Si:H contact. Assuming that N_D is uniformly distributed, then according to Poisson's equation the change in the electric field at the barrier will be given by [67]:

$$\Delta\mathcal{E} = \frac{q}{\epsilon} N_D L \tag{8.6}$$

where L is the device thickness. Consequently, the reverse voltage will exhibit a shift ΔV and the current decreases. Assuming $N_D \sim 10^{16} cm^{-3}$ and $\epsilon_s = 11.7$, the voltage shift (assumed to be $\Delta\mathcal{E}L$) due to this change in the electric field at the interface can be estimated as to be in the order of $0.1V$ for a film thickness $700 - 1000$Å, which is within the range of experimental observations. It is interesting to note that hole trapping has also been proposed to explain defect creation in reverse biased a-Si:H Schottky structures [124] and a-$SiN_x : H$ diodes [67].

The square-root time dependence of ΔV (Fig.8.7) also suggests that defect creation might also be associated with hole-electron recombination which has been proposed to account for light- or current-induced defect formation in a-Si:H thin films and diodes, where similar sub-linear kinetics were found (see §2.4 and §4.3 [13,14,54,67]. The defect creation rate is generally described by

$$\frac{dN_D}{dt} = Knp \tag{8.7}$$

where n and p are the electron and hole concentrations, and K is a constant. In light-induced defect generation, the product np is inversely proportional to the square of N_D. Therefore, N_D has a (1/3) time dependence with the illumination time. On the other hand, in the case of current-induced defect

creation, the current is carried mainly by one carrier (i.e.electrons) and the kinetics are different. A square-root time dependence of N_D is usually observed experimentally [14, 36]. This was explained by a model of electron-hole recombination, with the assumption that the hole concentration is proportional to the energetic electron current flowing into the anode [125]. The released recombination energy breaks weak Si-H bonds, and the freed hydrogen atoms then move to break weak Si-Si bonds leading to the generation of additional deep gap states. The newly-created defects in turn will reduce the life-time of carriers, and thus the recombination rate. Further defect creation due to recombination decreases, and saturation occurs. A similar model could be applicable to the present case of a-Si:H Cr-p^+-V devices, where a similar sublinear time dependence law is observed, although the details are different. The band diagram for a reverse-biased a-Si:H Cr-p^+-V diode is shown schematically in Fig. 8.26, with positive polarity applied to the top vanadium electrode. The symbol $\oplus$ denotes D^+ states. During stressing, electron-hole recombination occurs between electrons injected from the cathode (Cr electrode) and trapped holes in the valence band edge (indicated in the figure as process (a)). Another

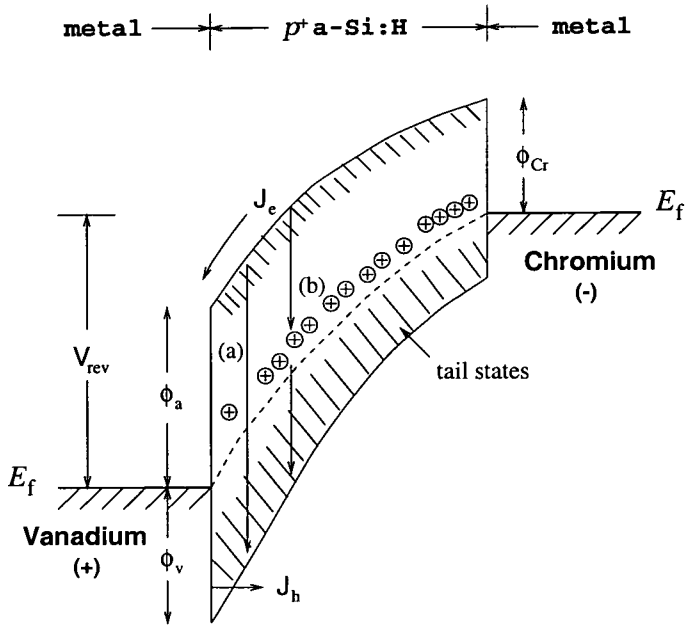


Figure 8.26: A schematic energy diagram for reverse biased Cr-p^+a-Si:H-V structures, where (a) represents band-tail electron-hole recombination, and (b) is recombination via $\oplus$ defects near E_F.

recombination path is via those charged $\oplus$ states near E_F (process (b)). The $\oplus$ states (D^+) also act as dominant trapping centres, and according to the DVAP doping model they are paired with ionised fourfold-coordinated dopants (B_4^-) [32,42]. Pairs of B_4^--D^+ states are equilibrated with electrically inactive threefold-coordinated structures (B_3^0) and neutral dangling bonds (D^0):

$$B_3^0 + D^0 <=> B_4^- + D^+ \tag{8.8}$$

Although recombination via this path is a two-stage process, the recombination rate could be very high because of the high density of defect states ($\sim 10^{18} cm^{-3}$ in the present case of $10^3 - 10^4 vppm$ doping). Moreover, the quasi-Fermi level is $\sim 0.2eV$ or less from the valence band edge due to the high doping. The $\oplus$ states are virtually located at the band tail, and trapped electrons thus have a high probability of recombining with trapped holes via tunnelling. The energy released by this recombination cannot be ignored. Due to electron-hole recombination, more D^0 states are created. In addition, the concentration of D^+ due to electron trapping decreases. As a result, more B_4^- states convert to a B_3^0. Assuming that the current mechanism during stressing can still be expressed by Eq.(3.3), the effective barrier height ϕ_{eff} is given by Eq.(3.6)

$$\phi_{eff} = (kT/q)[(\phi/E_0) - (V/E')] \tag{8.9}$$

where ϕ is the barrier height without tunnelling, and both E_0 and E' are related to the ionized dopant density $[B_4^-]$. With decreasing $[B_4^-]$, ϕ_{eff} increases, causing a reduction in device current. Fig. 8.27 shows the change of ϕ_{eff} against voltage for different stress conditions according to Eq.(8.9). The terms E_0 and E' are determined by fitting the J-V characteristic using Eq.(8.9) (see inserted figure) with varying ionised dopant density B_4^- (N_a) from $8.5 \times 10^{17} cm^{-3}$ (curve 1) to $6 \times 10^{17} cm^{-3}$ (curve 4), while keeping other parameters constant. These parameters are barrier height ϕ (0.72 eV), effective mass m^* (0.47 m_0), Fermi energy ($E_F - E_V$) (0.20 eV), and dielectric constant ϵ_r (11.7). Note that not only does the amplitude of ϕ_{eff} change with N_a but so does its slope

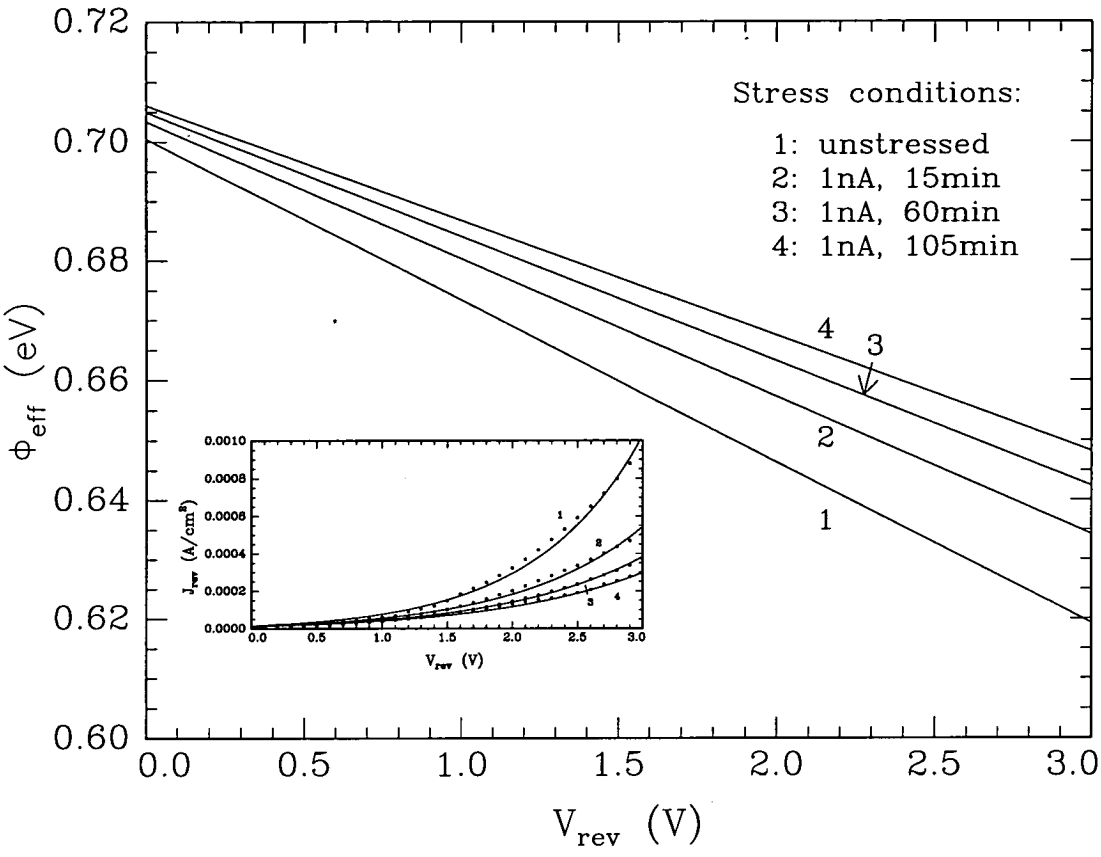


Figure 8.27: $\phi_{eff} vs. V$ for different stress conditions. The inserted figure shows the change in J-V characteristic with stress for a specimen (dot5-19, from Batch R430-4), where the solid lines are the fitted results using Eq.(8.9) (see text).

$(d\phi_{eff}/dV)$. The subsequent saturation in ΔV results from either a reduction in carrier lifetime due to the appearance of more and more D^0, and/or the filling of D^+ ($\oplus$) states, which reduces the available states for recombination and trapping. Both/either of them reduce(s) the defect-creation rate.

It should be pointed out that in the present case defect creation exhibits a current bias dependence ($J^{0.5}$, see Eq.(8.3)) which is different from that in either a-Si:H *pin* or metal-a-Si:H-metal (MSM) structures. As described in §4.3, in a-Si:H *pin* diodes the dependence of defect density on current bias is approximately $J^{1.5}$ [13], while in a-Si:H MSM diodes, it is linear with J [14,125]. It appears that defect creation in the present boron-doped structures tends towards saturation faster than in the other two structures containing an intrinsic or n-type layer. Although a systematic comparison between these

different structures cannot be made at this stage, it is not unreasonable to attribute the differences to different hydrogen diffusion coefficients, considering that the defect creation is a hydrogen-mediated process (as described in the early part of this section). It is known that hydrogen diffusion in a-Si:H is strongly doping-dependent [1, 2]. It is greatest in p-type and less in n-type material, compared with intrinsic a-S:H (see Fig.2.2). As a result, faster-moving hydrogen increases the rate at which weak Si-Si bonds are broken and thus also increases the generation rate of deep gap states. This in turn causes a faster reduction in the recombination rate.

The observed temperature dependence of the voltage shift ΔV, shown in Fig.8.8 and Fig.8.10, may be attributed to the thermally activated process in carrier trapping and de-trapping, and may also be related to the thermally activated hydrogen diffusion in films. In addition, it has been observed in most cases that defect generation in a-Si:H is a reversible process on thermal annealing at temperatures above $180°C$ [13, 53, 125]. In the present case of Cr/p^+/V thin films, annealing experiments were not attempted because temperatures over $100°C$ would cause oxidation of the top vanadium electrode and other unwanted effects.

At this point, it is interesting to compare the current instability in the Cr/p^+a-Si:H/V devices formed under constant current conditions with that occurring in voltage forming, as described in §4.2. In metal-p^+ni structures, as seen in Fig.4.6, when a voltage pulse is applied, the reverse current first reduces to a steady current which remains essentially constant. Only after a delay time t_d, does the current begin to increase, and it then rises almost instantaneously to its ON-state value. This feature was explained by a model for the switching operation of crystalline-silicon metal-p^+ni-metal (MISS) devices [11]. Holes injected from an increasingly forward-biased $p^+ - n$ junction accumulate at the $n - i$ interface, giving rise to a positive space charge in the vicinity of the metal-i interface and thus reducing the effective tunneling barrier. The abrupt increase in device current is the result of a substantial decrease in

the tunnelling barrier as the applied voltage increases further. In contrast, a continuous increase in the device current (or decrease in the resistance) in metal-p^+-metal structures was observed when biased with a voltage pulse (see Fig.4.8).

Experimentally, the current instability in the present case of constant current stressing is distinctly different to that observed in voltage forming. This will be discussed in detail in §8.4.3 of this chapter.

8.4.2 Post-stressing changes in conductance.

Changes in dopant coordination can also explain the observed post-stressing changes in device conductance shown in Fig.8.11. It is possible that the current stressing activates those electrically inactive but stable threefold-coordinated structures in p^+a-Si:H. Consequently, it leads to changes in band-tail carrier density Δn_{BT} and thus the hole current injected from the anode (V-electrode), as observed experimentally. A change in band-tail carrier density in doped a-Si:H has been observed and attributed to the activation of donor (or acceptor) states by means of an electric field or thermal-quench [47–50]. When the external stimulation was removed, a relaxation of the metastable state was usually found, due to the passivation of donor (or acceptor) sites, mediated by the migration of hydrogen atoms. The decrease in Δn_{BT} follows a stretched-exponential time dependence law as Eq.(2.6) [49,50]:

$$\Delta n_{BT}(t) = \Delta n_{BT}(0) exp[-(\frac{t}{\tau})^{\beta}] \tag{8.10}$$

where the relaxation time constant τ is thermally activated with an activation energy of $1eV$, and β is a dispersive factor. Similarly in the present case, once the stress is removed, the structural equilibrium requires those activated dopants to return back to their original states (threefold coordinated dopants). A relaxation process described by Eq.(8.10) thus occurs. The measured activation energy ($0.9 - 1eV$) is fairly close to that reported by others. Therefore,

the change in conductance reflects the relaxation in Δn_{BT}, although the exact relationship between them is not clear at the moment.

8.4.3 Forming mechanisms.

As shown in Fig.8.16, after ΔV reaches saturation a further increase in the current bias causes the eventual forming of the device. As pointed out above, the kinetics of defect generation at lower bias exhibits a sub-linear relation with stress time, which could be explained qualitatively by a model based on electron-hole recombination. The microscopic cause of the defect creation is attributed to the bond breaking of weak Si-Si and Si-H bonds, with the mediation of hydrogen. However, since electron-hole recombination is a self-limiting process, with increasing bias, the recombination rate decreases gradually due to a lower capture cross section and/or carrier density. Alternative mechanisms might prevail at this stage. The average field across the specimen is enhanced with the increase of current bias, as measured by V_{mea} (or V_0), and under such a high field, energetic (hot) electrons be generated. According to Nieuwesteeg *et al*, the condition for the appearance of hot electrons is given by [14]

$$\mathcal{E} > \frac{\epsilon_{loss}}{\lambda_e} \tag{8.11}$$

where $\mathcal{E}$ is the electric field, ϵ_{loss} ($\sim 103meV$) is the energy loss at each collision when electrons drift to the anode, and λ_e is the mean free path of electrons. Using the value determined experimentally, $\lambda_e \sim 1.5\ nm$ [14], thus the required field strength $\mathcal{E} \sim 7 \times 10^5 V/cm$. In present case, near forming ($V_0 = 10 - 14V$), the average field applied to the device reaches values as high as $\sim 2 \times 10^6 V/cm$ (for device thickness of 700 $\sim$ 1000 Å). In the barrier region, e.g.at the V-a-Si:H contact (anode), the field may be even higher due to the existence of the highly resistive barrier. Therefore, it is expected that large numbers of hot electrons exist under an increasing current bias. These hot electrons can result in direct dangling bond formation if the kinetic energy of the electron

is high enough to break a Si-H bond. In addition, hot electrons that drop to the Fermi level of the metal at the anode bring about a large release of energy [equal to $(kT_{eff}+q\phi_a]$, where T_{eff} is an effective electron temperature), leading to further breaking of Si-Si and Si-H bonds. Fig. 8.28 shows the schematic representation of the process. In the case of unstressed devices (a), carrier transport through the p^+a-Si:H layer is essentially uniform. With increasing current stress, local defects could develop along those transport path where microscopic irregularities or uneven heating exist, which reduces the device current (b). The damage is particularly severe in the interface near the anode

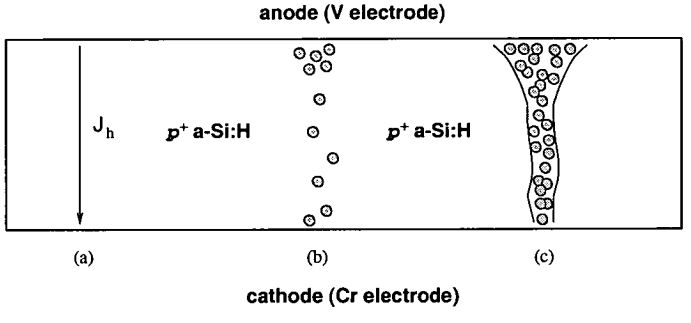


Figure 8.28: Schematic representation of the forming model. (a) Unstressed condition. (b) Formation of defect islands due to the breaking of large numbers of Si-Si and Si-H bonds within a-Si:H layer. (c) Further increasing the stress bias leads to those defect islands linking and creating a continuous filamentary conduction path.

for most weak bonds locate in the interfacial region and also the highest field strength exists there. One consequence would be the diffusion of vanadium metal from the anode into the bulk a-Si:H. When the bias exceeds the critical current those defects in the bulk and the interface link into a chain and thus form a filamentary path (c), and therefore the device current increases rapidly. Obviously, the filamentary path has lost its dielectric properties with respect to the original a-Si:H material. It is interesting to note that a similar mechanism has been proposed to account for breakdown in SiO_x dielectric films [126,127].

It is worth noting that the formation of a conducting filament is also seen in these Cr-p^+a-Si:H-V structures after voltage-biased electro-forming [22,23]. Moreover, under either voltage pulses or constant current forming specimens

exhibit a metal-non metal transition [128], which provides extra information about the filament. In the analysis later in *Chapter* 9 it is shown that the microstructure of the filament in formed Cr/p^+a-Si:H/V devices could indeed be modelled as an heterogeneous medium composed of metallic inclusions in an insulator host. The metallic inclusions originate from the diffusion of the top vanadium electrode during the forming process.

Chapter 9

Metal-Non Metal Transitions and the Conducting Filament.

A metal-non metal (MNM) transition has been observed in Cr/p^+a-Si:H/V structures formed by constant current stressing or by voltage-biasing. It has been induced EITHER by varying the temperature OR by changing the resistance of the memory ON-state into which the device is first formed or is subsequently programmed by voltage pulses. In this *Chapter*, the basic experimental results on the MNM transition are first described and analysed, and then related to the conducting filament in formed a-Si:H memory devices. Analogue switching is analysed in terms of the activated tunnelling mechanism.

9.1 Results on the temperature-induced MNM transition.

9.1.1 DC Characteristics.

Fig. 9.1 shows the logarithm of the dc resistance as a function of temperature for three devices showing the MNM transition. Above and below a transition temperature, T_{tr} (defined as the temperature at which the minimum resistance occurs), there are two fundamentally different regimes of temperature dependence, indicating metallic and semiconducting behaviour respectively. The variation in T_{tr} $(60 - 100K)$ among different samples is probably caused by slight differences in the micro-structure formed in the devices. On the

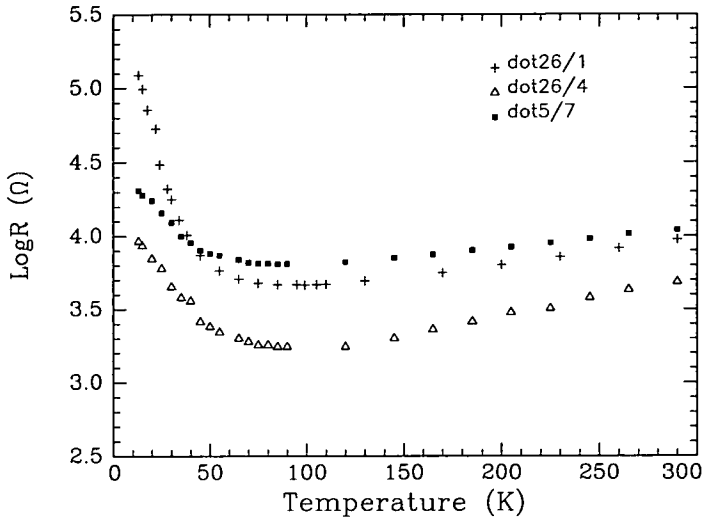


Figure 9.1: The logarithm of the dc resistances as a function of temperature for three samples (samples from Batch 10070/14).

semiconductor side of the MNM transition (below $60K$), there are two temperature regions where conduction is characterised by two activation energies: in the range of $1.18-6.29meV$ at $20-60K$, and $0.22-2.49meV$ when $T < 20K$.

Above T_{tr} the resistances increase slightly with increasing temperature, showing metallic behaviour, and the resistance *vs* temperature curve can be best described by the following empirical relationship:

$$R(T) = A + B(T - T_{tr}) + C(T - T_{tr})^2 \quad (for\ T > T_{tr}) \tag{9.1}$$

where A, B, C are constants depending on the sample. The temperature coefficient of the resistance, TCR, defined by $\alpha_T = (1/R_0)dR/dT$ (where R_0 is the resistance at $273K$), is in the range of $3 - 5 \times 10^{-3}K^{-1}$.

The differences occurring in ΔE, T_{tr}, and the positive TCR among different samples probably arise from the nature of the electro-forming process. Although the devices under test originated from a single batch, and thus have the same doping level and p^+ layer thickness, the current densities (or voltage pulses) required to form the samples show some variation. Thus the forming process, driven by different current densities (or voltage pulses), could lead to

slightly different microstructures in the filament.

The dynamic resistance, (dV/dI), also exhibits an interesting change around T_{tr}, as shown in Fig. 9.2. Below $55K$ (dV/dI) around zero bias exhibits a peak

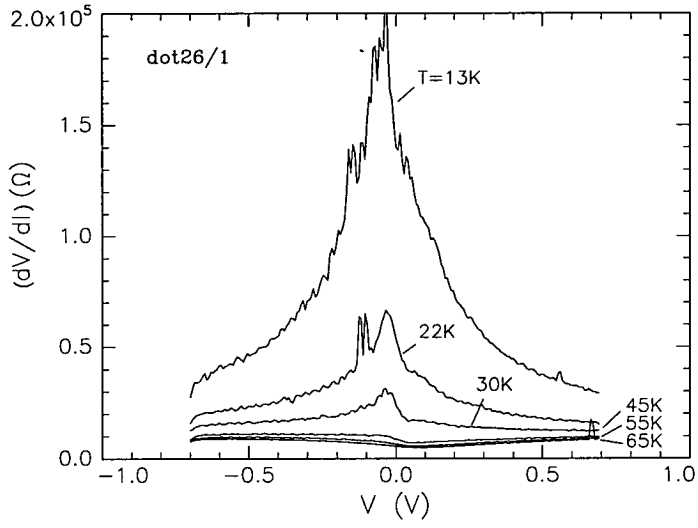


Figure 9.2: Dynamic resistance (dV/dI) *vs.* voltage at temperature range $13-65K$ (samples from Batch 10070/14).

which is slightly on the negative voltage side and decreases with increasing temperature. Above $65K$, the peak changes into a minimum centred slightly to the positive side of zero bias. The zero-bias dynamic conductance, (dI/dV) at $V = 0$, denoted $G(0,T)$, is found to decrease with temperature in a parabolic way, as shown in Fig. 9.3. A non-zero value of $G(0,T)$ when $G(0,T)$ is extrapolated to the zero temperature may be associated with the background parallel conduction path in the material surrounding the filament. It is interesting to note that a resistance peak was also found in other formed metal/a-Si:H p^+ni/metal structures (see Fig.4.4 for an example) [9] and has been widely reported in various thin granular metal films at very low temperature [17, 129]. This provides further evidence that the microstructure of the filament is associated with a metallic material of some sort.

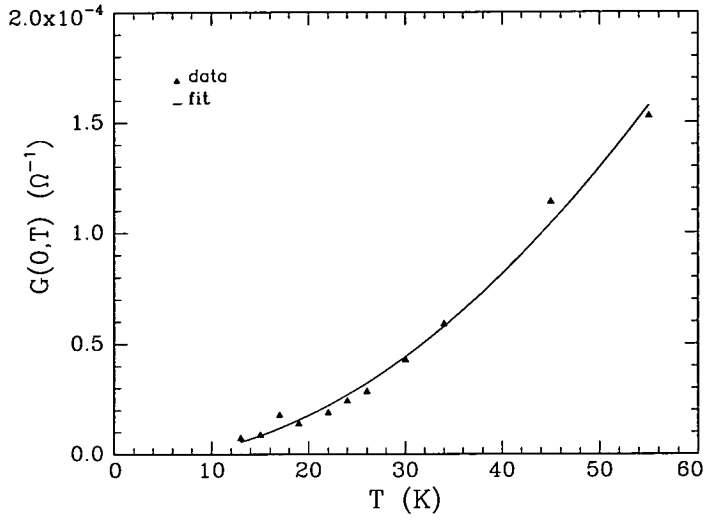
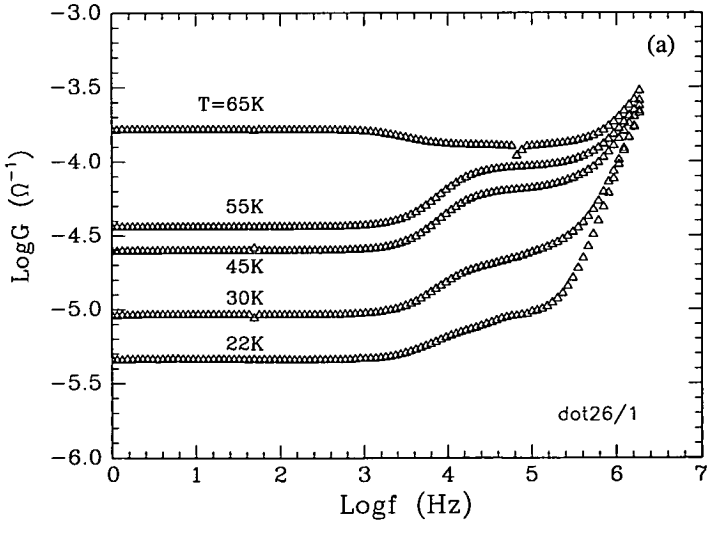


Figure 9.3: Temperature dependence of zero-bias dynamic conductance G(0,T) at low temperature. The solid line is the fit of data to the empirical formula $a_T + b_T T + c_T T^2$ (device as in Fig.9.2).

9.1.2 AC Characteristics.

Figs. 9.4(a) and (b) show the ac conductance $G(\omega)$ and capacitance $C(\omega)$ (both on a *Log*-scale) as a function of frequency at different temperatures. In the frequency range $10^3 - 10^4 Hz$, both $G(\omega)$ and $C(\omega)$ show distinctive changes. The ac behaviour is capacitive at temperatures $\leq 55K$, but it changes rather drastically at temperatures over $55K$. The capacitive relaxation disappears, the ac conductance $G(\omega)$ decreases with increasing frequency, and at the same



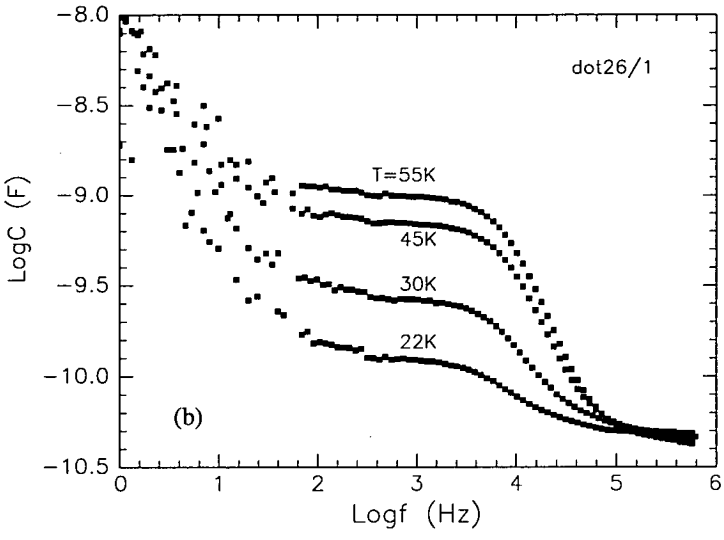
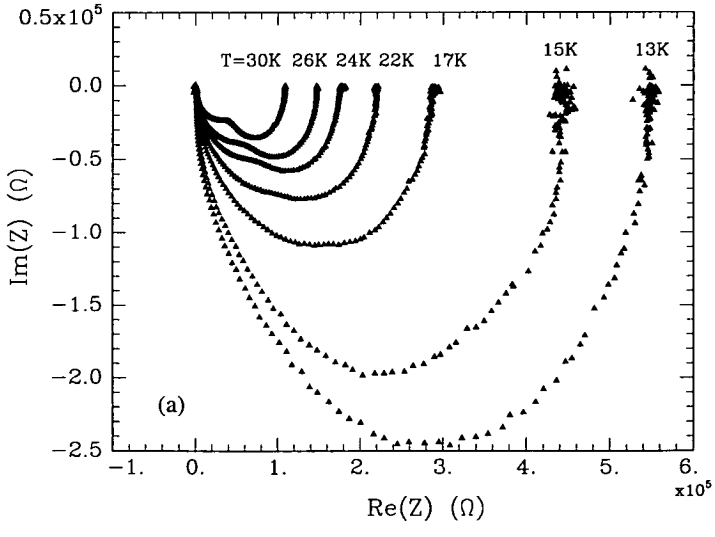


Figure 9.4: $LogG(\omega)$ (a) and $LogC(\omega)$ (b) vs. frequency at different temperature (sample from Batch 10070/14).

time, $C(\omega)$ becomes negative (not shown in the Fig.9.4(b)), indicating the onset of an inductive effect. This transition is more clearly shown in the form of complex plane plots as illustrated in Figs. 9.5(a) and (b). Below the transition temperature ($T \leq 55K$), $Im(Z)$ lies in the negative quadrant of the impedance plane (Fig.9.5(a)). There is a well-defined semicircle at temperatures below about $20K$, a distinctively capacitive behaviour for semiconductors or insulators. The single semicircle starts to evolve into two as temperature rises. The two semicircles become most distinct around $T \sim 55\,K$ as shown in Fig.9.5(b). Once the temperature is over about 65 K, the larger relaxation



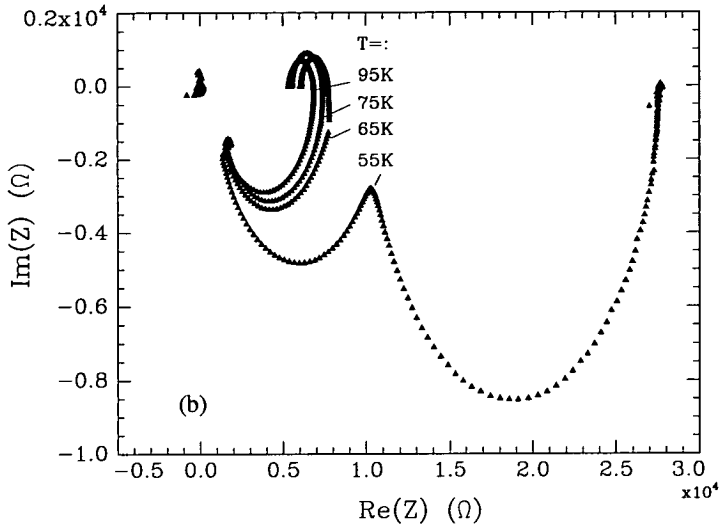


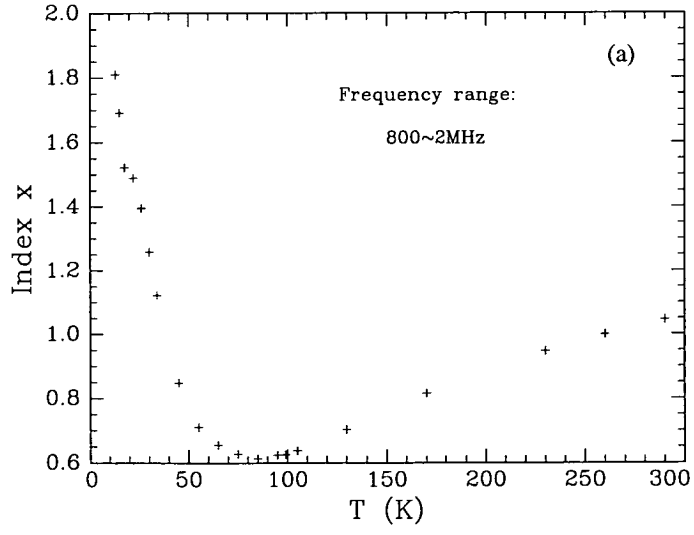
Figure 9.5: Cole-Cole plot of impedance data (device as in Fig.9.4).

in the lower frequency range completely disappears and a new semicircle is formed in the positive quadrant, i.e. an inductive effect develops.

It can be seen also from Fig.9.4(a) that the frequency dependence of $G(\omega)$ in both high $(800KHz - 1MHz)$ and low $(10^3 - 10^4 Hz)$ frequency regions follows a power law:

$$G(\omega) \propto \omega^x \tag{9.2}$$

Over the temperature range of $13 - 300K$, the index x in the high frequency



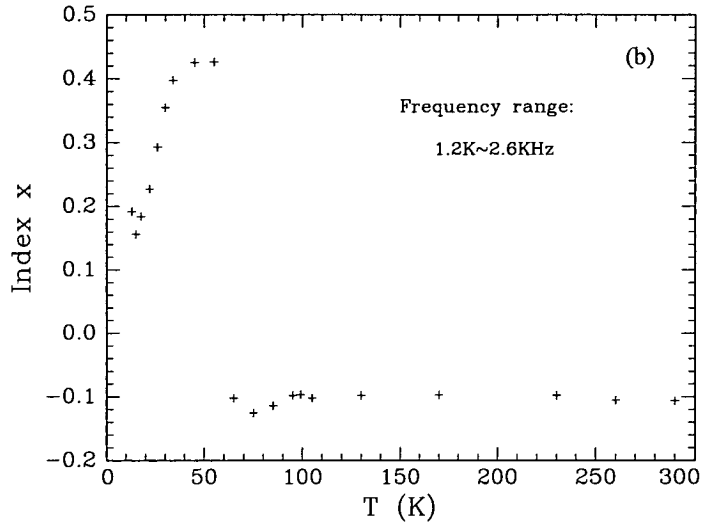
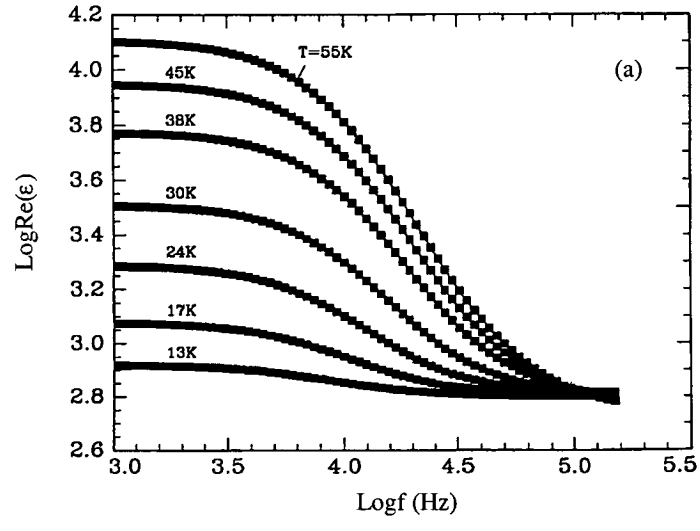


Figure 9.6: Change of the index x with temperature in (a) high frequency region $800KHz-2MHz$, and (b) low frequency range of $1.2KHz-2.6KHz$.

region changes with temperature systematically. This is shown in Fig. 9.6(a), where x decreases first from near 1.8 at $13K$ to a minimum value of 0.61 at $\sim 85K$ and then rises again to ~ 1 at room temperature. In the *low* frequency range (see Fig.9.6(b)), x first increases from 0.156 at $15K$ to 0.426 at $55K$ and then changes sign to almost a constant negative value, i.e.~ -0.10 above $60K$. It is found that the dielectric constant $\epsilon(\omega)$ in the corresponding frequency regions also obeys a power-law:

$$\epsilon(\omega) \propto \omega^{-y} \tag{9.3}$$



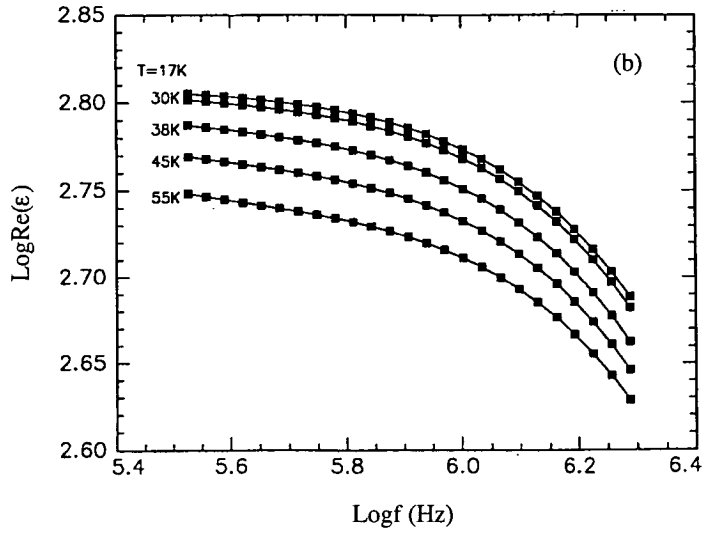


Figure 9.7: Frequency dependence of $\epsilon(\omega)$: (a) at low frequency; (b) at high frequency (device as in Fig.9.4).

The temperature dependence of $\epsilon(\omega)$ in both the low and high frequency ranges are shown in Figs. 9.7(a) and (b) respectively. The exponent y at the low frequencies shows a systematic increase with temperature, from 0.120 to 1.18, while at high frequencies, y is almost constant at 0.350 ± 0.015.

It is interesting to note that near the transition temperature T_{tr} the sum of x (the conductance exponent) and y (the dielectric constant exponent) in the high frequency region is close to unity. For example, $x(T = 65 - 100K) = 0.61$ and $y(T = 55K) = 0.35$, respectively, giving $(x + y) = 0.96$; while in the low frequency region, although $y < 0$ when $T \geq 65K$, $x(T = 65 - 100K) = -0.10$ and $y(T = 55K) = 1.18$, thus $(x + y) = 1.08$. This suggests that the metal-non metal transition in the present case could be of a percolation-like type. Percolation theory predicts that near the percolation threshold p_c $G(\omega, p)$ and $\epsilon(\omega, p)$ of a random mixture should obey a power-law behaviour, and the exponents x (for $G(\omega, p_c)$) y (for $\epsilon(\omega, p_c)$) should satisfy $(x + y) = 1$ [98].

9.2 The metal-non metal transition as a function of memory resistance.

A metal-non metal (MNM) transition is also observable when the room temperature analogue memory resistance R_m is switched between different resis-

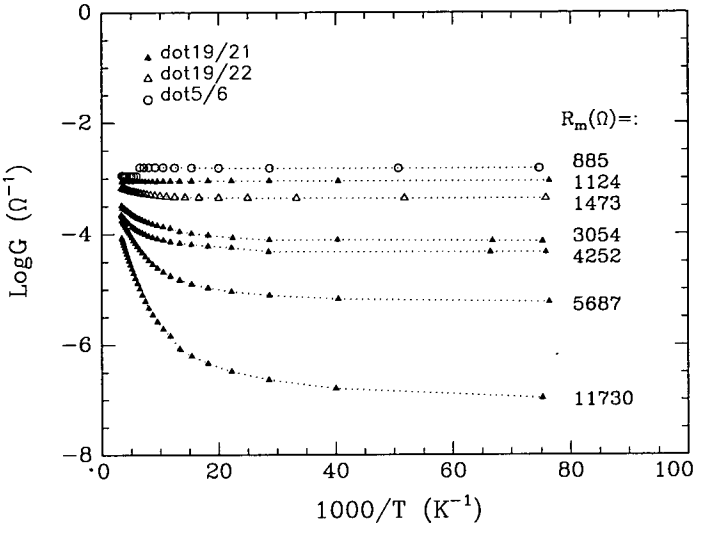


Figure 9.8: *LogG vs.*$1/T$ with temperature in the range $13 - 300K$ (samples from Batch 10070/14).

tance states. For the present purpose the 'memory resistance' is defined as the resistance measured at 0.1 V and 300K. In Fig. 9.8 the logarithm of conduct-

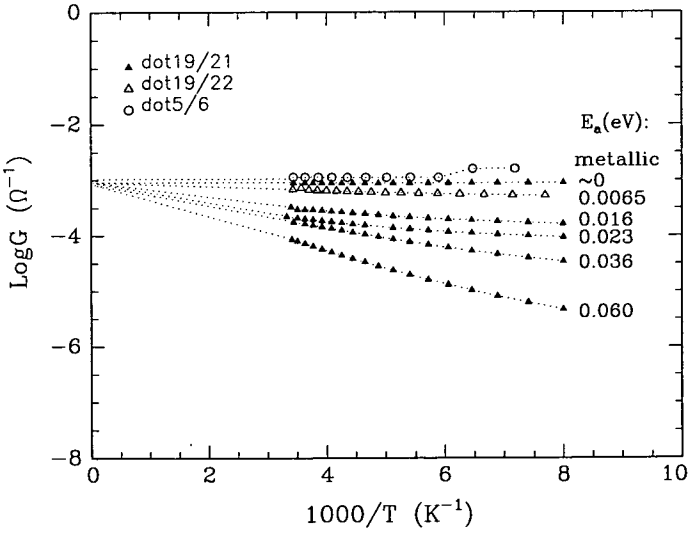


Figure 9.9: *LogG vs.*$1/T$ (temperature range $150 - 300K$) (samples as in Fig.9.8).

ance (G) is plotted against inverse temperature for a range of analogue memory states. The conductance shows a transition from an activated process in the higher resistance states to metallic behaviour for values of R_m lower than $\sim 1000\Omega$. The activation energies in the non-metallic states can be determined from the higher temperature region ($150K - 300K$), where the plot of $LogG\ vs. 1/T$ exhibits a linear relation, more clearly shown in Fig. 9.9. Table

$R_m(\Omega)$	$\Delta E(eV)$	**Intercept** $LogG(0)$
11730.3	0.06	-3.04
5686.7	0.036	-3.15
4521.5	0.023	-3.29
3054	0.016	-3.19
1473	0.00653	-3.05
1247.9	0.00483	-3.01
1124	0.000633	-3,04
1053	no activation	-3.04

Table 9.1: Change of ΔE with memory resistance

9.1. summarises the values of the room temperature resistance R_m of the different analogue memory states, the activation energy ΔE, and the intercept $LogG(0)$ on the conductance axis. A near-linear relation between ΔE and $LogR_m$ is observed as shown in Fig. 9.10, which is similar to results reported

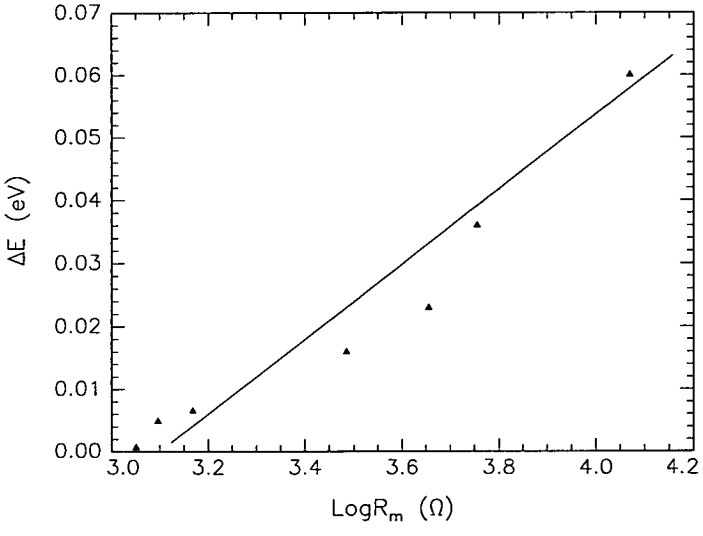


Figure 9.10: $\Delta E\ vs. LogR_m$. The solid line is for guiding the eyes.

by others (see for example Fig.4.3) [8]. Note that the magnitude of ΔE in the highest memory resistance state ($R_m = 11730.3\Omega$) is $0.06eV$, which is significantly lower than expected for heavily doped p^+-amorphous silicon ($\Delta E \sim 0.2eV$).

The dynamic resistance of memory states (dV/dI), also measured at low temperatures, is shown in Fig. 9.11 for results measured at $25K$. The dynamic

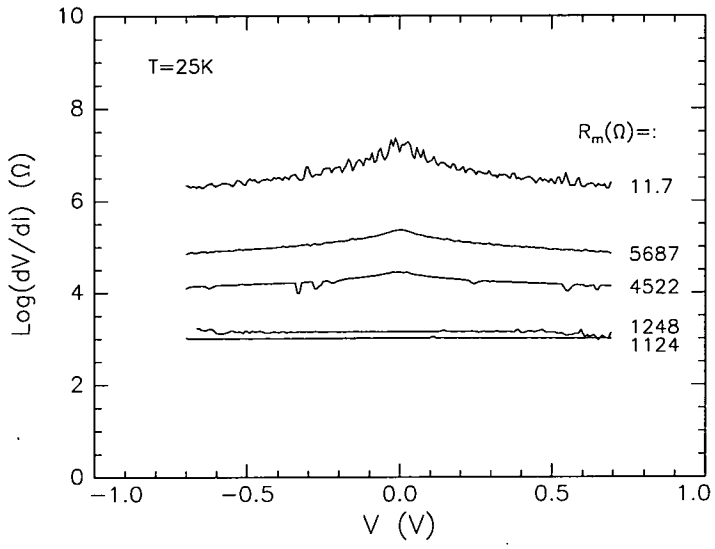


Figure 9.11: Log(dV/dI)$vs.V$ for different memory resistances at $25K$ (samples as in Fig.9.8).

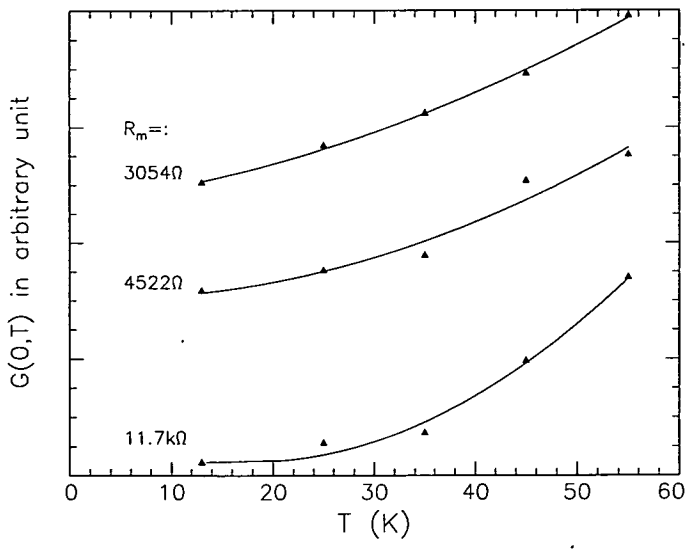


Figure 9.12: $G(0,T)$ $vs.$ T in a range $10-60K$ for different memory resistances (samples as in Fig.9.8).

resistance (dV/dI) exhibits a peak centred about zero volts and the peak changes systematically with memory resistance R_m, reducing as R_m approaches $\sim 1K\Omega$. It also changes with temperature in a similar manner as in the case of temperature-induced MNM transition. Fig. 9.12 shows $G(0,T)$, the zero-bias dynamic conductance *vs.* temperatures for various R_m. It must be emphasised, however, that here the change in (dV/dI) is brought about by a change of memory resistance, instead of temperature.

9.3 Analysis and discussion.

9.3.1 Equivalent circuits.

The ac impedance spectra presented in §9.1.2 have been simulated by a complex non-linear least square (CNLS) procedure [130], in which the sum of the squared differences S between the measured and simulated dispersion is minimised with respect to adjustable parameters, a_j ($j = 1...m$), of the model circuit dispersion relation. In this way, an optimised fit of an equivalent circuit to the measured data can be obtained. Fitting quality can be checked by either the relative error for individual parameters (i.e.R and C), or by plotting the residuals, ΔRe and ΔIm, against the logarithm of frequency. These residuals should be distributed evenly around the horizontal axis. Figs. 9.13 (a) and (b) show the simulation results at $T = 55K$ and $T = 85K$ respectively, and the corresponding equivalent circuits for $T \leq 55K$ and $T \geq 65K$.

Tables 9.2 and 9.3 list the relative errors for results at $T = 30K$ and $T = 85K$ respectively. The relative errors are found to be less than 3% in a temperature range $20 - 300K$. The temperature dependence of the relative errors in the range $13 - 55K$ is shown in Fig. 9.14. Below $20K$, R, R_1 and C, particularly rise significantly. This may result from a strong inter-relationship among these parameters in this temperature range.

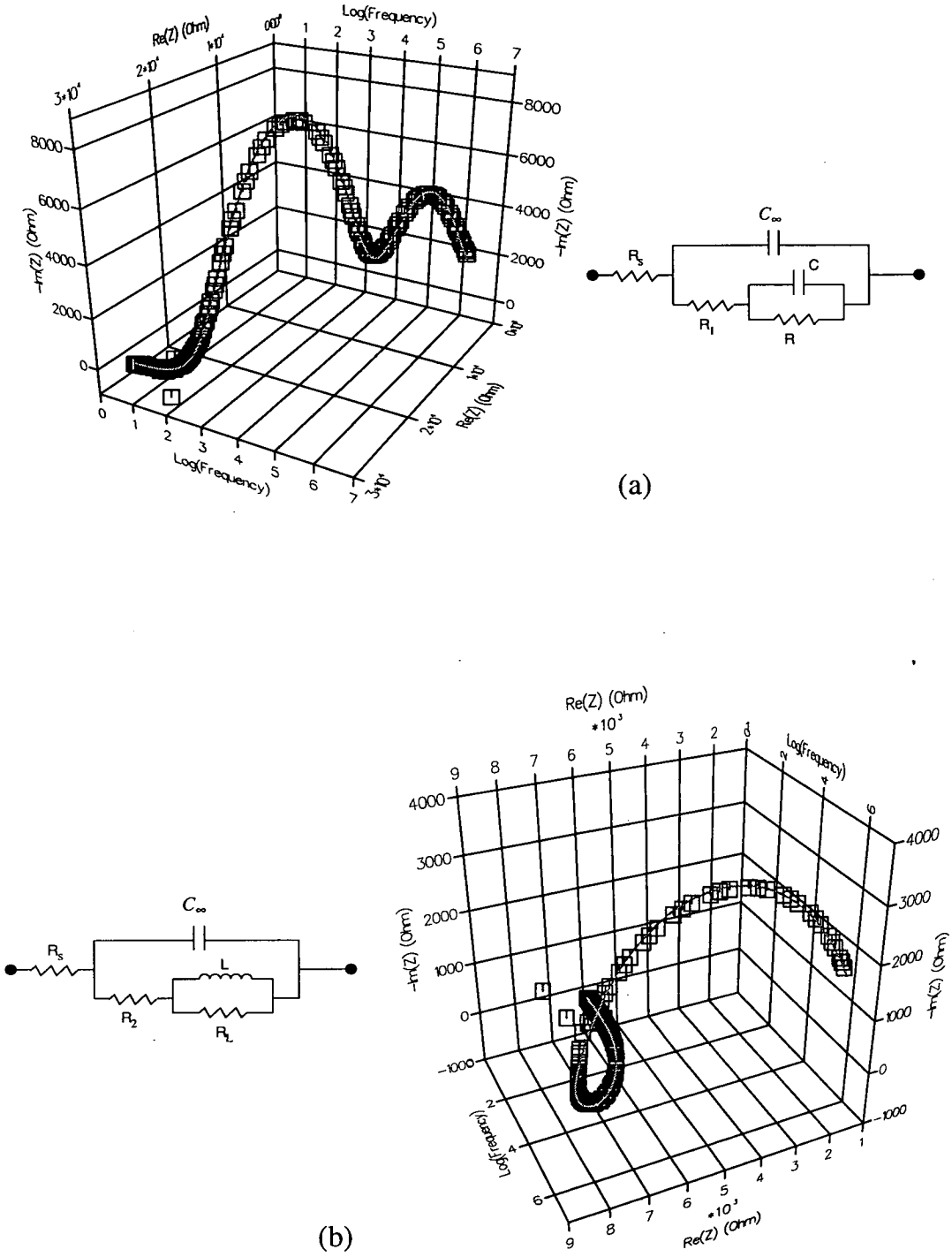


Figure 9.13: The simulation results (lines) at $T = 55K$ (a) and $T = 85K$ (b), and the corresponding equivalent circuits for $T \leq 55K$ and $T \geq 65K$ respectively. Data is represented as open squares (device as in Fig.9.4).

Parameters	Fitting values	Re.errors (%)
R_s	$916.5(\Omega)$	2.93
C_∞	$51.2(pF)$	0.66
R_1	$44.31(k\Omega)$	0.29
R	$62.99(k\Omega)$	0.92
C	$580.9(pF)$	2.36

Table 9.2: Relative error for the fitting at $T = 30K$.

Parameters	Fitting values	Re.errors (%)
R_s	$1101(\Omega)$	1.16
C_∞	$51.66(pF)$	0.55
R_2	$4438(\Omega)$	0.33
R_L	$1867(\Omega)$	0.67
L	$77.49(mH)$	1.88

Table 9.3: Relative error for the fitting at $T = 85K$.

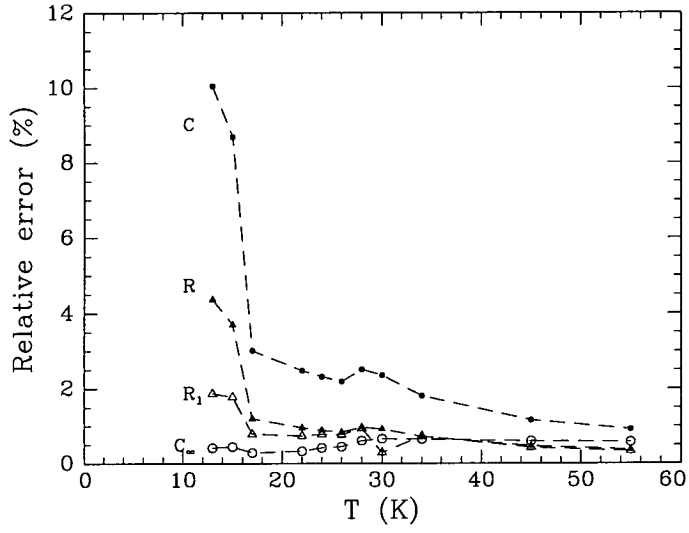


Figure 9.14: Temperature dependence of relative error of some fitting parameters in a range of $13 \sim 55\ K$.

The frequency dependence of the residual errors at $30K$, ΔRe and ΔIm, are shown in Fig. 9.15 (a). Both approach zero at low frequencies ($< 1kHz$). With increasing frequency, ΔRe and ΔIm oscillate around the zero axis, but the magnitudes of ΔRe and ΔIm are limited to about 6%. The large increase in ΔRe above $1\,MHz$ is due to the effect of contact resistance. It is found that

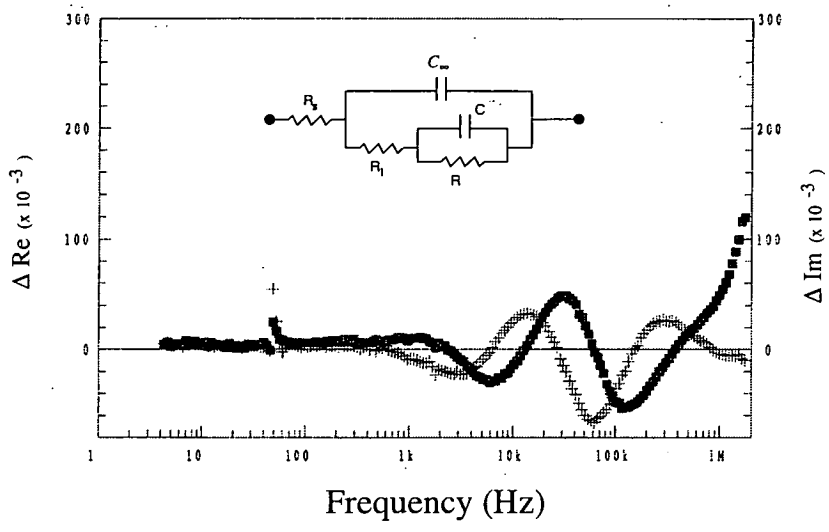


Figure 9.15: Frequency dependence of relative errors for ΔRe (solid square) and ΔIm (cross) at $30K$. In (b) improved curves are illustrated after adding another $R'C'$ branch to the circuit shown in (a).

the oscillations at high frequency can be further minimised by adding another $R'C'$ branch to the equivalent circuit, as shown in Fig.9.15(b), but this leads to a large increase in the relative errors (i.e.$\sim$ 8%) for both R' and C'.

9.3.2 Filament structure.

There is little direct evidence about the constitution of the conducting filament in formed devices. All that is known for certain is that during forming some of the top vanadium contact diffuses and/or electromigrates into the a-Si:H (see §4.2.2 [8,24]). It is interesting to note that the temperature coefficient of the resistance TCR ($3-5\times10^{-3}K^{-1}$) of those devices showing MNM transitions is fairly close to the corresponding values for vanadium in the temperature range $100-300K$ ($4.513\times10^{-3}K^{-1}$) [131], and also to that for VSi_2 ($3.51\times10^{-3}K^{-1}$) [132]. This implies that the metallic conduction occurring above T_{tr} could be closely associated with the presence of vanadium, or vanadium compounds (e.g. VSi_2) introduced into the a-Si:H material during the forming process. For the present discussion, the idealised model of the filament first proposed by Hajto *et al* [10], as described in §4.1.4, is assumed to be appropriate and for convenience a schematic diagram of the filament in Fig.4.5 is reproduced here as Fig. 9.16. Note that Jafar and Haneman have recently used and developed

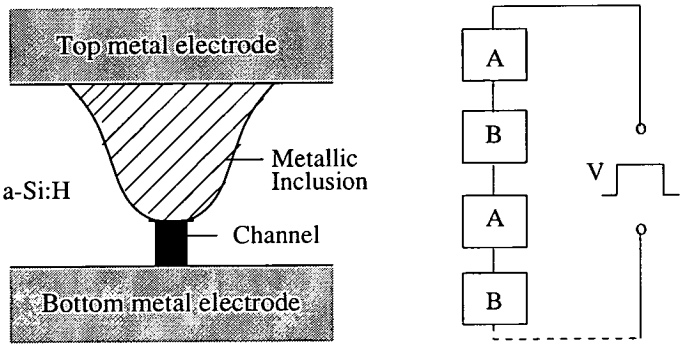


Figure 9.16: Schematic diagram of filamentary structure in a formed a-Si:H memory device (from Hajto *et al* [10]).

a very similar model (see §4.1.4 [24]). The assumption is that the filament consists of a single metallic inclusion extending from the top contact (V), with a narrow channel connecting it to the bottom contact (Cr). The evidence is that the overall dimension of the filament at the top contact is $< 0.5\mu m$ [22].

The length of the channel must be consistent with tunnelling and electron confinement sufficient to cause the observed quantised resistance, eg. about $50\mathring{A}$ [10].

It should be clear from the discussion in *Chapter* 4 that there is a good deal of indirect evidence for the basic features of the model but the precise nature of the metallic inclusion and the channel are unknown. The metallic inclusion could consist simply of a finely divided (ie nanoscale) dispersion of vanadium metal particles in an a-Si:H matrix, as suggested by Jafar and Haneman [24]. It seems equally likely, however, that reactions are induced between the vanadium and the environment resulting in the formation of vanadium silicides and even, possibly, borides, oxides, and hydrides. Indeed, recalling that high temperatures are involved during electroforming (see §4.2.2), it would be surprising if compound-forming reactions did not occur. Any such compounds formation could result in a uniform metallic inclusion in the a-Si:H or, again, in a dispersion within an a-Si:H matrix. In what follows the terms "metallic" or "metallic inclusion" are used in a general sense to cover the variety of possibilities.

The physical meaning of the fitting parameters introduced in the last section (including resistances, capacitances, and inductances) can be understood on the basis of the microstructure shown in Fig.9.16. The circuits in Fig.9.13 are now converted into the reduced ones shown in Fig. 9.17, with the terms R^*, C^* in (a) and $R_L{}^*$, L^* in (b) being related to the fitting parameters.

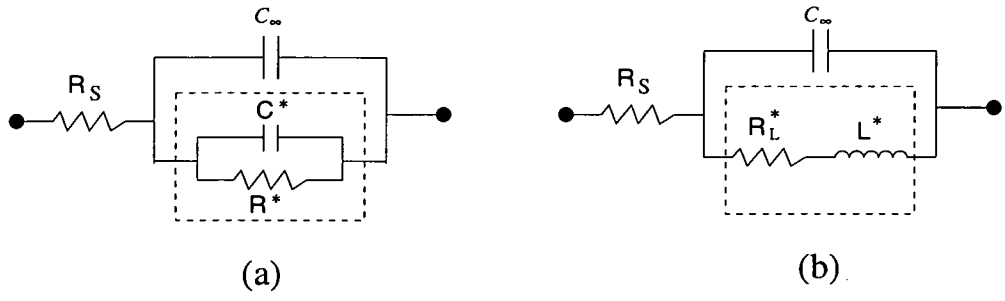
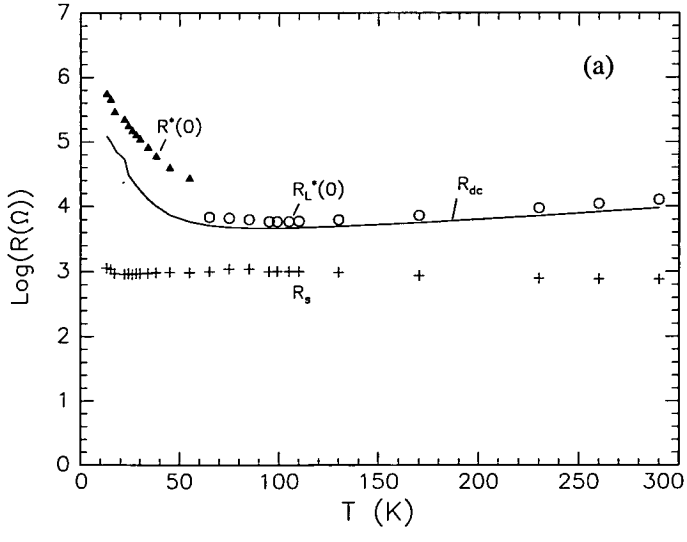


Figure 9.17: Equivalent circuits derived from those in Fig.9.13. (a) for $\leq 55K$ and (b) for $T \geq 65K$.

The circuit elements in Fig.9.17(a) and (b) may be related to features in the microstructure of the filament shown in Fig.9.16 as follows: R_s is a contact resistance between the electrodes and the filament, while C_∞ is probably a function of the semi-conducting media surrounding the filament; $R_L{}^*(0)$ is associated with the bulk resistance of the metallic particles embedded in the filament (note that it increases with temperature in an identical manner to the dc resistance-see Fig.9.18(a)), while $R^*(0)$ could be the 'gap' resistance between metallic particles and $C^*(0)$ the capacitance associated with $R^*(0)$; L becomes apparent at higher temperatures (i.e. $T > T_{tr}$), where the filament becomes metallic, and thus probably arises from the interaction among various metallic conduction paths [$R^*(0)$, $R_L{}^*(0)$ and $C^*(0)$ are denoted as the values of $R^*(\omega)$, $R_L{}^*(\omega)$ and $C^*(\omega)$ at zero frequency].

Figs. 9.18(a) and (b) show the temperature dependence of all three resistances R_s, $R^*(0)$ and $R_L{}^*(0)$, and the two capacitances $C^*(0)$ and C_∞, in the range $13 - 300K$. For comparison, the measured dc resistance (solid line) is also illustrated in Fig.18(a). Both R_s and C_∞ are almost constant over the whole temperature range. Before and after the metal-non metal transition $R^*(0)$ and $R_L{}^*(0)$ exhibit a very similar dependence on temperature as the dc resistance R_{dc}. At high frequencies and low temperatures (i.e. before the transition), the ac resistance increases with temperature, as shown in Fig. 9.19, and that is attributable to the space (capacitance) between metallic particles being effec-



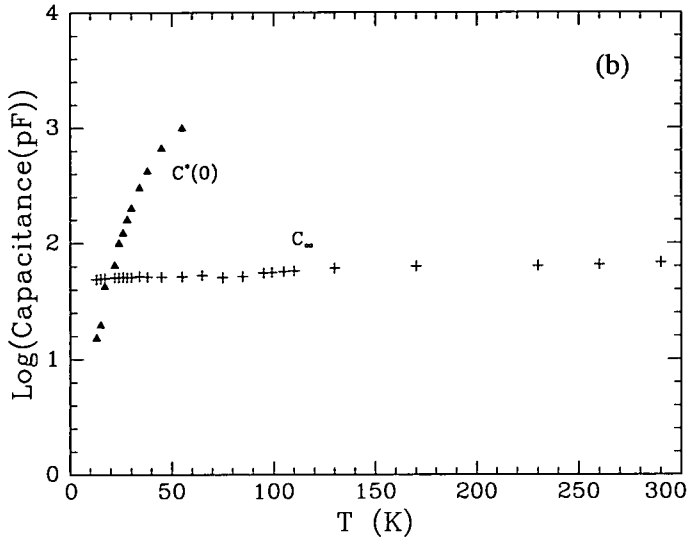


Figure 9.18: Temperature dependence of terms R_s, $R^*(0)$ and $R_L{}^*(0)$ (in (a)), and $C^*(0)$ and C_∞ (in (b)). The solid line in (a) represents the measured dc resistance.

tively short-circuited by the ac signal. As a result, the ac resistance is much lower than the dc resistance R_{dc} (solid triangles), and it increases with temperature. With increasing temperature, R_{dc} reduces rapidly and near the transition temperature, the ac resistance starts to merge with R_{dc}. It is interesting

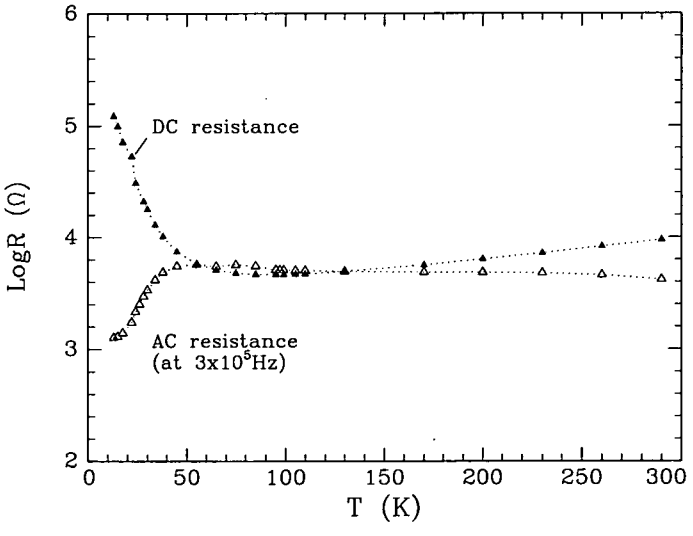


Figure 9.19: Temperature dependence of the logarithm of ac resistance (open circles) at $3 \times 10^5\, Hz$. DC resistance (solid triangles) is illustrated for comparison.

to note that this characteristic is very similar to the ac characteristics of dis-

continuous metallic films, shown in Fig.5.3 in § 5.1. This is another indication that the filament is very likely a metal-containing structure.

It is noted from Fig.9.18(b) that $C^*(0)$, associated with the gap resistance $R^*(0)$, shows an extraordinary increase from about 15 pF at $13K$ to about 1000 pF at $55K$ as the temperature approaches the MNM transition from the semiconductor side, and then becomes effectively zero at temperatures $> 55K$. This anomaly may reflect a change in the dielectric properties of the filament near the metal-non metal transition, and it is discussed in detail in the next section.

9.3.3 Effective dielectric constant of the filament.

The effective dielectric constant $\epsilon_{eff}(\omega)$ when $T < T_{tr}$ can be deduced from the ac characteristics, that is, $\epsilon'(\omega) \equiv Im[Y(\omega)/\omega C_0]$. From Fig.9.13(a) (or Fig.9.17(a)) the admittance $Y(\omega)$ of the equivalent circuit when $T \leq 55K$ is given by:

$$Y(\omega) = \frac{R_1 + R + R_1(\omega CR)^2}{(R_1 + R)^2 + (\omega CRR_1)^2} + j\left[\omega C_\infty + \frac{\omega CR^2}{(R_1 + R)^2 + (\omega CRR_1)^2}\right] \quad (9.4)$$

where C_0 is the geometric capacitance (ie, without the metallic particles) and C is derived from the circuit in Fig.9.13(a). In Eq.(9.4) the series resistance R_s is ignored since it has a negligible effect on the main characteristics. The effective static dielectric constant ($\omega = 0$) is thus:

$$\epsilon_{eff} = \epsilon'(0) = \frac{C_\infty}{C_0} + \frac{C}{C_0}\frac{R^2}{(R_1 + R)^2} \quad or \quad \epsilon_{eff} = \frac{C_\infty + C^*(0)}{C_0} \quad (9.5)$$

where $C^*(0) = CR^2/(R_1 + R)^2$. Equation (9.5) directly relates ϵ_{eff} with the capacitance $C^*(0)$ or C. Substituting the data for C, C_∞, R, and R_1 from the equivalent circuit into Eq.(9.5), the changes of ϵ_{eff} vs temperature are shown in Fig. 9.20. The effective dielectric constant ϵ_{eff} changes from about 836 at

$13K$ to nearly 13612 at $55K$, or ϵ_{eff} increases by a factor as high as 16. These results suggest that the anomalous change in C (or $C^*(0)$) is associated with the change in ϵ_{eff} of the filament material.

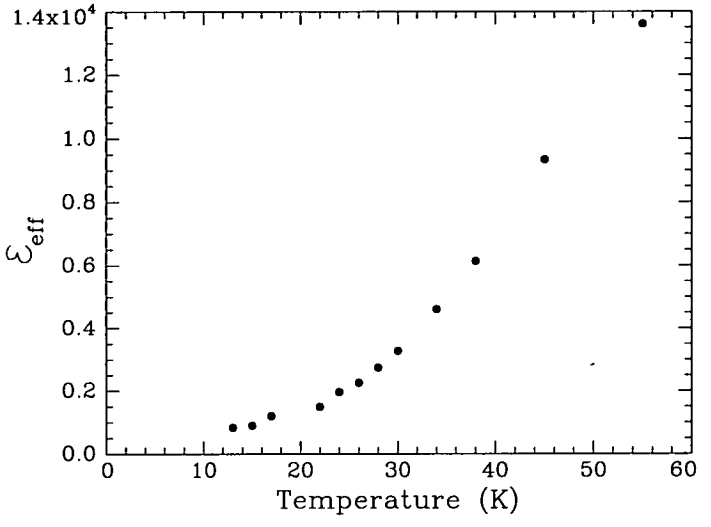


Figure 9.20: Change of ϵ_{eff} with temperature (sample as in Fig.9.8).

9.3.4 The enhancement of ϵ_{eff}.

As described in §5.2, the anomalous increase in dc dielectric constant near a metal-non metal transition has been widely observed in various granular metallic thin films [100]. The enhancement of the dielectric constant is normally associated with an increase in the metallic component p in conductor-dielectric mixtures. When p reaches a threshold p_c, the dielectric constant of these materials usually exhibits a notable increase. In the present case of a temperature-induced MNM transition, it is possible that the temperature may affect the distribution of metallic particles embedded in whatever constitutes the host material of the conducting filament, so that ϵ_{eff} shows an anomalous change. The ac characteristics have indicated that a MNM transition of this type might be associated with a percolation-like transition (see §9.1.2). It is thus proper to use the percolation theory introduced in §5.2 to describe ϵ_{eff}. In this way, the change in ϵ_{eff} can be correlated with the microstructure of the filament. According to Eq.(5.3),

$$\epsilon_{eff} = \epsilon_h \mid \frac{p - p_c}{p_c} \mid^{-q} \tag{9.6}$$

where q is the critical exponent; $q \sim 0.75$ and ~ 1.3 for three- and two-dimensional heterogeneous conductor-dielectric binary composites respectively; ϵ_h is the dielectric constant of the host material, and p and p_c are the volume fraction of the particles and the threshold concentration respectively. Assuming that the conducting filament has a cylindrical shape, and the embedded particles are spheres with the radius r, then ϵ_{eff} can be related to the spacing s between particles and their radius r:

$$\epsilon_{eff} = \epsilon_h \mid \frac{kr^3/(s+r)^3 - p_c}{p_c} \mid^{-q} \tag{9.7}$$

where k is a constant. The dimension of the embedded particles can be estimated from the activation energy. Electron transport in the filament containing metallic particles is assumed to be an activated tunnelling process. The activation energy ΔE is related to the particle radius r by [86]:

$$\Delta E = \frac{e^2}{4\pi\epsilon r} \tag{9.8}$$

where $\epsilon = \epsilon_0\epsilon_s$. Using experimental data of $\epsilon_s = \epsilon_{eff}$ (~ 1000) and $\Delta E = 1.2 - 6.2meV$, the radius of the particles is in the range of $2.9 - 15$Å. Assuming that the conducting filament has a three dimensional structure with a critical index of 0.75 and, in addition, treating the critical volume filling factor as an adjustable parameter, the change of $(\epsilon_{eff}/\epsilon_h)$ with s for different r is shown in Fig. 9.21, where $p_c = \pi/6$. As expected, the effective dielectric constant increases with a decrease in the separation of particles, and it goes asymptotically to infinity as s approaches zero. The relative change of the effective dielectric constant has almost the same magnitude as that found experimentally, i.e. for particles with a radius of 6Å, $(\epsilon_{eff}/\epsilon_h)$ increases from ~ 1.07 to 15.8 when s decreases from $\sim 7\mathring{A}$ to $\sim 0.05\mathring{A}$, compared to the increase of $(\epsilon_{eff}/\epsilon_h)$ from 1 to 16 experimentally. Therefore, the enhancement

of ϵ_{eff} is well explained in terms of a percolation-like critical behaviour of the dielectric constant, which goes asymptotically to infinity at the threshold p_c. In the case of two-dimensional structure, a similar relation between $(\epsilon_{eff}/\epsilon_h)$ and s can also be obtained.

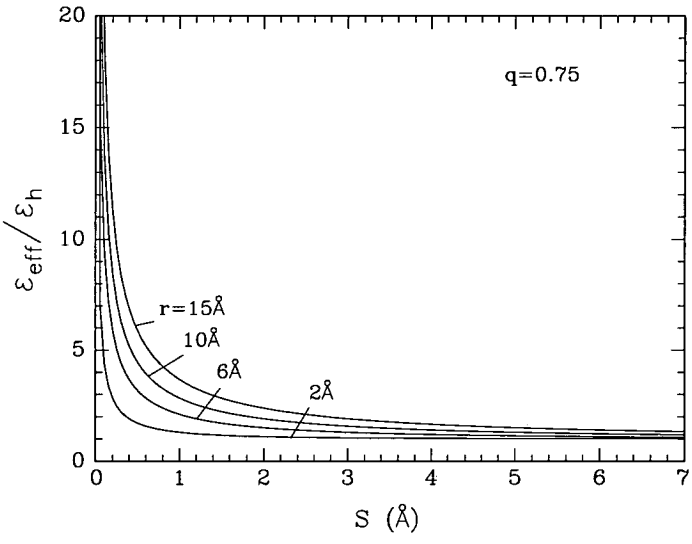


Figure 9.21: Change in $\epsilon_{eff}/\epsilon_h$ with s for the radius range $2 - 15$Å.

9.3.5 MNM transitions associated with memory resistance.

It can be seen from Table 9.1 that the values of ΔE decrease, approaching zero as the memory resistance R_m decreases (R_m has been defined previously in §9.2). The magnitude of ΔE in the highest memory resistance state ($R_m = 11730.3\Omega$) is $0.06eV$ and is significantly lower than expected for p^+-amorphous silicon ($\sim 0.2eV$). According to the model suggested for the MNM transition in heavily doped semiconductors [133] the small activation energies for non-hopping conduction, which are of the same order, might be associated with delocalization of some electronic states at the Fermi energy E_F. This process is described theoretically as an Anderson transition due to the overlapping of two Hubbard bands at the Fermi energy. If the activation energy ΔE is defined as

$$\Delta E = E_C - E_F \tag{9.9}$$

where $(E_C - E_F)$ is the energy separating localised electronic states from extended ones, then the activation energy should go linearly to zero at the MNM transition. In the present case, however, the MNM transition is initiated by changing the resistance of the sample using voltage pulse programming and not by changing the composition, as is usually the case for doped semiconductors.

The value of $G(0) \sim 1 \times 10^{-3}\Omega^{-1}$ (see Table (9.1)) is approximately the same value for all resistance states, yielding the conductance corresponding to the metal-non metal MNM transition. A value of conductivity σ cannot be obtained from the measurements because the geometry of the active area (i.e. of the conducting filament) cannot be determined directly. However, using the expression for minimum metallic conductivity given by Mott [39]:

$$\sigma_{min} = 0.026e^2/\hbar a \tag{9.10}$$

and assuming a spherically symmetrical structure (coordination number=6) with an interatomic distance between metallic sites of $a = 3\text{Å}$, $\sigma_{min} = 210\ \Omega^{-1}cm^{-1}$. Using that value with $a = 3\mathring{A}$ and the minimum metallic conductance value of $G(0) \approx 10^{-3}\Omega^{-1}$ (from the experiments), an active area $A = 150 \times 10^{-15}cm^2$ is obtained for the conducting filament, corresponding to a diameter of $44\mathring{A}$. This again indicates that the conduction mechanism in the analogue memory states is associated with very small geometries, perhaps down to atomic dimensions. For other types of MNM transitions (i.e. when the effective coordination number is not necessarily equal to 6) the value of σ_{min} can be different. Experimental data on MNM transitions observed in VO_x and $La_{1-x}Sr_xVO_3$ suggest that σ_{min} is about $1000\Omega^{-1}cm^{-1}$ [134]. Kikuchi [135] and Mott [136] have also calculated σ_{min} in the case of heavily doped n-type semiconductors without compensation, and concluded that σ_{min} has a value of $\sim (0.1e^2/\hbar a)$ because of the smaller effective coordination number involved. These considerations do not invalidate the suggestion of very small dimensions regarding the geometry. A higher value of σ_{min} implies even smaller dimensions.

9.3.6 Comparison of the two MNM transitions.

Although the temperature-induced MNM transition (Fig.9.1) and the memory resistance related MNM transition (Fig.9.9) appear different and may be initiated by different physical processes, there are notable similarities between them. For example, in both cases, the activation energy of conductance near the transition (from the semiconductor side) is almost same. In the former, it is in several milli-electron volts (i.e. $\Delta E = 1.18 - 6.29meV$ at $20 - 55K$), while in the latter it is $6.53\ meV$ when the memory resistance R_m reduces to about $1473\ \Omega$ (Table 9.1). Both are much smaller than expected for p^+-amorphous silicon (e.g. $\sim 0.2eV$). In addition, a zero-bias dynamic resistance peak occurs in both, and it increases as the device deviates from the transition either with decreasing temperature (Fig.9.2) in the former, or with increasing R_m in the latter (Fig9.11). In particular, the temperature dependence of the zero-bias dynamic conductance exhibits a similar parabolic reduction at low temperatures (Fig.9.3 and Fig.9.12). These similarities indicate that there might be a very similar microstructure in the conducting filament of both type of device, in which metallic particles (i.e. the top vanadium) are embedded into the p^+a-Si:H matrix due to the forming process. The difference between these two type of transitions probably arise from different particle sizes or possibly the geometry of the filament.

9.4 Activated tunnelling mechanisms and switching.

9.4.1 Transport mechanisms in the filament.

In §9.3.2 it was suggested that the conducting filament can be treated as a structure with metallic particles embedded in a non-metallic host matrix. Electron transport in the filament is therefore inevitably modified by the existence of these particles, and may follow a similar mechanism to that found in granular metal films (or discontinuous metal films). As discussed in *Chapter* 5, in such

a system, carrier transport is dominated by electron tunnelling between the metallic particles, instead of tunnelling directly between electrodes. Adding an electron to a particle is an activated process, because the transference leads to a change in the electrostatic potential or Coulomb energy of the particle. Evidence for such a mechanism can be seen in various electrical properties. For example, it is almost always found that there is a much lower activation energy in formed devices, as shown in Fig.9.9 (or Table 9.1), usually in the range of a few to few tens of meV, similar to those in granular metal films [86,137].

Moreover, the dynamic resistance (dV/dI) observed at low temperatures (see for example, Fig.9.2) usually exhibits a peak centering at or near zero bias, systematically changing with either temperature, also fairly similar to those reported for granular metal films. This could be attributed to the well-known Coulomb blockade effect associated with ultrasmall metallic particles in an insulating medium. The charging energy of a particle is given by:

$$E_{ch} = \frac{e^2}{2C_m} \tag{9.11}$$

where C_m, the particle capacitance, depends on the size of particles. Assuming that the particles have a spherical shape with a radius in the order of $\sim 10\mathring{A}$, yield $C_m \sim 10^{-18}F$, and a corresponding E_{ch} of $\sim 60\ meV$, which is larger than the thermal energy kT in the experimental temperature region (usually below $300K$).

9.4.2 Analogue changes in device resistance.

It is interesting to ask how electronic switching is affected by the metal-containing structure suggested in the previous analysis? From the discussion in previous subsections it is concluded that charge transport in such a system should be dominated by an activated tunnelling process, in which electrons tunnel via metallic particles. The conductivity σ is given by [138]

$$\sigma \sim exp(-A\phi^{1/2})exp(-\frac{\Delta E}{k_B T}) \tag{9.12}$$

where A is a constant related to particle spacing, ΔE, the activation energy, is the work required to transfer a charge between metallic islands, and ϕ is the potential barrier between islands. This equation shows that the $Ln\sigma$ is proportional to the inverse of temperature, as observed in most experiments (see for example, Fig.9.9). In addition, the low activation energies observed can be qualitatively explained in terms of the particle size r to which ΔE is related by $(e^2/4\pi\epsilon r)$. In analysing the high dielectric constant in §9.3.4, this form of activation energy has already been used to estimate the particle size from known activation energies.

In order to analyse the switching phenomena quantitatively, it is necessary to discuss the activated tunnelling in further detail. Consider the idealised filament structure shown in Fig.9.16(b) and the corresponding energy diagram for three collinear particles in an applied electrical field, shown in Fig. 9.22.

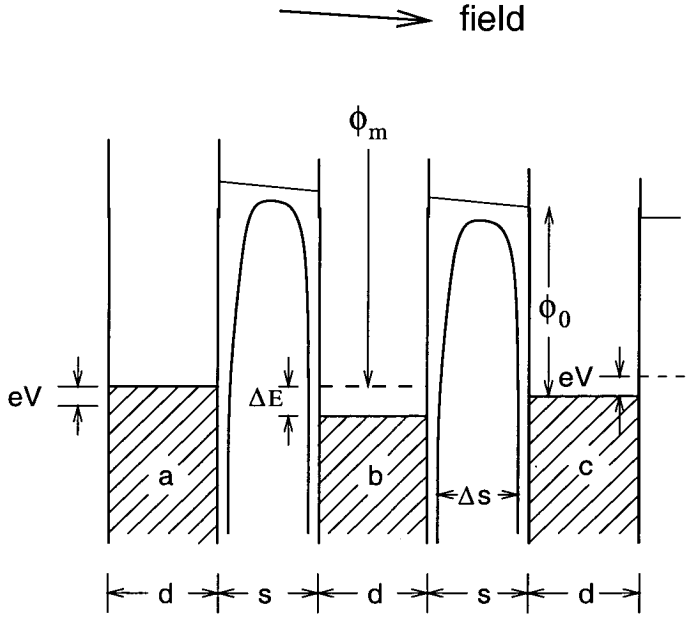


Figure 9.22: Energy diagram for a three-particle array.

The Fermi energy of particle b is ΔE below that of particles a and c. A field applied to the electrodes will displace the relative Fermi levels by eV. The em-

bedded metal particles a, b, and c (material 'A') are assumed to be distributed uniformly in the filament and have a spherical shape with an average radius r ($= d/2$), separated from other particles by an average distance s. The current flowing through a single gap of unit area between particles will be

$$J(V,T) = e\int_0^\infty N(T,E)D(E_X)dE \tag{9.13}$$

where e is the charge on an electron, $N(T,E)$ is the supply function proportional to $\int f_b(f_a - f_c)dE$ (f_i is the Fermi function of particle i, $i = a,b,c$), and $D(E_X)$ is the transmission coefficient, depending exponentially on the distance s between particles. For $eV \ll k_BT$, according to Hill, Eq.(9.13) can be solved to give [139],

$$J(V,T) = \frac{8\pi me}{h^3B^2}sinh(\frac{eV}{k_BT})\frac{\pi Bk_BT}{sin\pi Bk_BT}exp(-A\overline{\phi}^{1/2})exp(-\frac{\Delta E}{k_BT}) \tag{9.14}$$

when $\Delta E > k_BT$, and

$$J(V,T) = \frac{8me}{h^3B^2}sinh(\frac{eV}{k_BT})\frac{(\pi Bk_BT)^2}{sin\pi Bk_BT}exp(-A\overline{\phi}^{1/2})\frac{k_BT}{\Delta E} \tag{9.15}$$

when $\Delta E < k_BT$, where $B = (A/2\overline{\phi}^{1/2})$, and $\overline{\phi}^{1/2}$ is the average barrier height. The term ΔE represents the activation energy, suggesting a thermally activated tunnelling process in the case of $\Delta E > k_BT$, but the temperature dependence is modified by the tunnelling term $(\pi Bk_BT/sin\pi Bk_BT)$. When $\Delta E < k_BT$, the conduction is not an activated process, and the temperature dependence is mainly due to that of tunnelling. It is noted that at very small bias, $sinh(eV/k_BT) \rightarrow eV/k_BT$, and Eq.(9.14) converts into Eq.(9.12).

The activation energy $\Delta E = (e^2/4\pi\epsilon r)$, where $\epsilon = \epsilon_0\epsilon_{eff}$, was initially proposed by Neugebauer and Webb who assumed a hemisphere-like particle and neglected the interaction between particles [86]. Swanson *et al* later included image effects when calculating the amount of work which must be done in

transferring an electron from one particle to the other. They gave the following formular for ΔE [140]:

$$\Delta E = \frac{e^2}{4\pi\epsilon}\frac{1}{r}[1 + \frac{r}{s} + (\frac{r}{s})^2 + (\frac{r}{s})^3 + 2(\frac{r}{s})^4 + 3(\frac{r}{s})^5 + ...]^{-1} \tag{9.16}$$

This equation suggests that ΔE changes with the spacing or tunnelling distance between metallic particles, s. Fig. 9.23 shows the calculated results for change to ΔE with s.

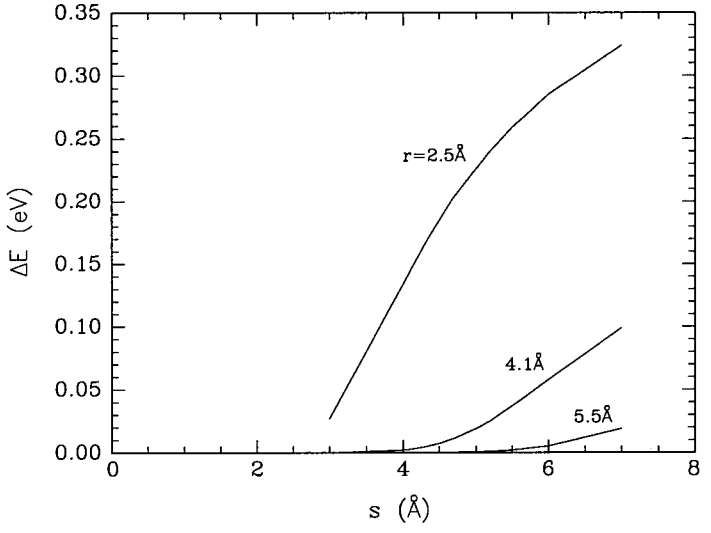


Figure 9.23: ΔE *vs.* s for different particle sizes of 2.5, 4.1 and 5.5Å.

The calculated spacing dependence of the memory resistance, R_m, determined by Eq.(9.14) and Eq.(9.15), is illustrated in Fig. 9.24. The activation energy ΔE is chosen from Eq.(9.16). In the calculation the diameter of the filament is taken to be $50\mathring{A}$, and $\epsilon_h = 11$. The average barrier height $\overline{\phi}^{1/2}$ is replaced by ϕ_I, the barrier height which includes image forces and derived by Simmons [141]. It is seen that R_m decreases steadily with decreasing s. For example, at $300K$ it changes from $5.6\,M\Omega$ (corresponding to an OFF state) to a $1600\,\Omega$ ON-state when s reduces from $7\mathring{A}$ to about 4Å.

These results show that a change in s causes a change not only in R_m, but also in ΔE, as ΔE changes with both r and ϵ_{eff}. From the analysis of the MNM

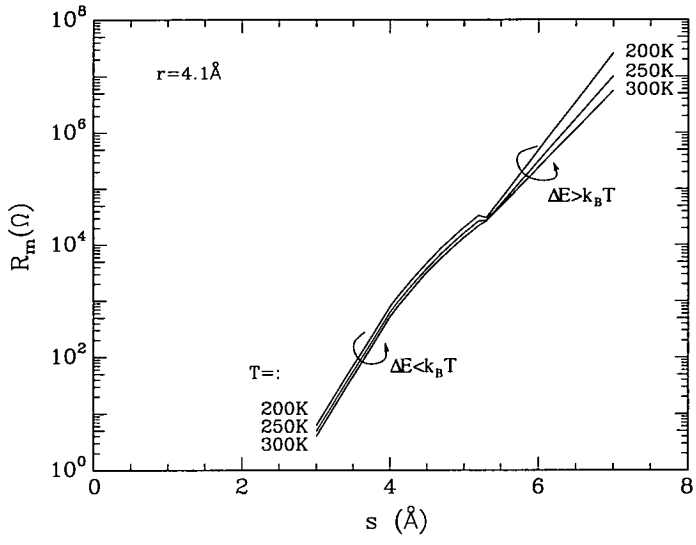


Figure 9.24: R_m *vs.* s at three temperatures $200K$, $250K$ and $300K$. Particle radius r is assumed to be 4.1Å.

transition in §9.3.4, it is known that the effective dielectric constant ϵ_{eff} of the filament changes with the spacing between particles. On decreasing s, ϵ_{eff} increases and thus ΔE reduces. As a result, it is expected that the filament will appear more conductive. When s increases, ϵ_{eff} decreases and ΔE increases, and so does the device resistance. This is consistent with the experimental observations.

In addition, from Fig.9.24 it can also be seen that in the regime of thermally-activated tunnelling, where $\Delta E > k_B T$, R_m appears more thermally activated at a high memory resistance state than it is at a lower resistance state. This difference results merely from the change in s. It is understandable if one looks at the variation in ΔE shown in Fig.9.23 which shows that a large particle spacing results in a larger ΔE compared with a smaller s, thus leading to a high resistance state, as experiments shows.

The change in transport mechanisms can also account for the dynamic resistance characteristics shown in Fig.9.11 where (dV/dI) rises with an increasing R_m. In a high R_m state, electrons tunnel mainly via metallic particles by thermal activation. The size of the particles affects the electron tunnelling and the zero-bias dynamic resistance could be the result of a Coulomb block-

ade effect due to an extremely small particle size. On decreasing R_m, electron tunnelling becomes less temperature-dependent (as indicated by a reducing ΔE). The separation of particles s becomes comparable with the particle size and J increases as more empty states becomes accessible in the metallic particles. As a result, the zero-bias (dV/dI) due to the Coulomb blockade reduces.

In Fig. 9.25 calculated $\Delta E\, vs. Ln R_m$ curves are shown to compare with experimental results. The dashed line is calculated using $\Delta E = (e^2/4\pi\epsilon r)$, which

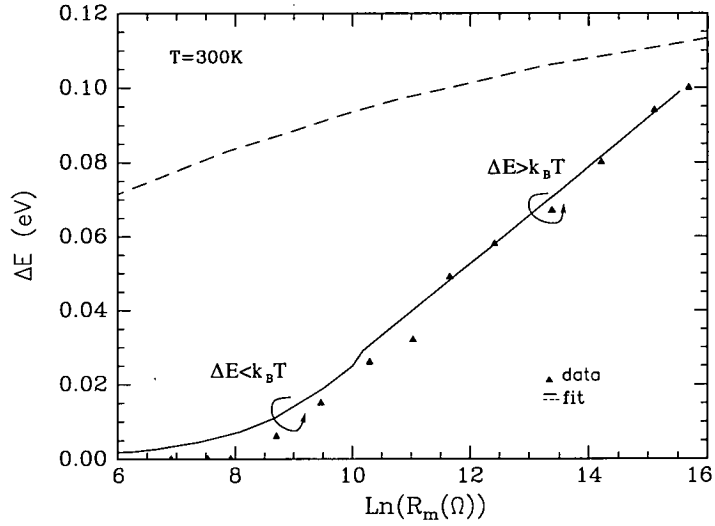


Figure 9.25: $\Delta E\, vs. Ln R_m$. The solid and dashed lines are calculated results according to Eq.(9.14) ($\Delta E > k_B T$) and Eq.(9.15) ($\Delta E < k_B T$), but using different forms of the activation energy (see text).

gives a rather large activation energy. The solid line represents a much better fit using Eq.(9.16). The fairly good agreement between the model and experimental data in the later case suggests that the effect of the image forces cannot be excluded. There might be a strong interaction between particles and charges in such a system. The calculations also show that when ΔE reduces from values appropriate to high resistance memory states, where $\Delta E > k_B T$, into low ones where $\Delta E < k_B T$, the barrier height changes significantly, from $1.7eV$ to $0.9eV$, coincident with the change in transport mechanism, i.e. from an activated tunnelling process to a less temperature-dependent tunnelling.

The observed linear I-V characteristic near the ON-state may result from that large drop in $\overline{\phi}$.

The question arises why s changes under an external electric field. That is not known at this stage. It is interesting to note however that a similar assumption about changes in memory resistance being associated with s has been suggested by other workers [10,24]. One possible reason, as Jafar *et al* proposed, could be that there is a positive charge on the embedded metallic inclusions or particles in the conducting filament. They noted that analogue switching characteristics are always associated with p^+ a-Si:H. Positive charges are thus likely to be trapped at the interface between a metal and a-Si:H. The charged particles could be moved slightly under a sufficiently high electric field. It was suggested that this electromigration of particles causes the changes in s, which in turn leads to an observable change in R_m or ΔE. According to their estimation particles in the filament as a whole could gain enough acceleration in a very short duration of $10ns$ (a typical switching time) [24].

Chapter 10

Conclusions.

10.1 Introduction.

This final chapter draws together the experimental and theoretical results presented in *Chapter* 7,8, and 9, and summarises the main contributions of this study. Suggestions are also made for further research.

10.2 Achievements of the work.

1) Current transport in unstressed reverse-biased Cr/p^+a-Si:H/V devices is controlled mainly by thermionic-field emission of carriers over the V/p^+a-Si:H barrier. The barrier width, according to an analysis of the barrier profile, is in the region of $90 - 100\mathring{A}$ for barrier heights ranging from $0.1eV$ to $1eV$. Comparisons are obtained from fitting measured I-V characteristics to a model equation. With increasing voltage bias, the effective barrier height decreases due to tunnelling. As a result, the device current is enhanced with increasing reverse voltage.

2) In the initial stages of electro-forming by constant current stressing, with increasing injection of charge, via either increasing bias or time, the device current exhibits a unique instability different from that in the voltage forming process. The current usually decreases with an increasing stress bias and time. This is interpreted in terms of the creation of defects in the a-Si:H. It is possible that the trapping of injected holes may cause a change in the

electric field near the interface, and hence result in a shift in device current. It is also proposed that the defect creation is mainly due to electron-hole recombination within the a-Si:H since the defect generation rate, as measured by the voltage shift ΔV at a constant current in the $I - V$ curve, is found to follow a square-root time-dependent law. The energy released by electron-hole recombination breaks weak Si-H bonds and the freed hydrogen atoms move to break weak Si-Si bond, leading to the generation of additional deep gap states. In addition, current stressing may alter the thermal equilibrium existing between ionised fourfold-coordinated dopants (B_4^-) and electrically inactive threefold-coordinated boron atoms (B_3^0), causing the passivation of some B_4^- and thus increasing the density of mid-gap states. In both cases, the newly-created defects will reduce the lifetime of carriers, and will also reduce the recombination rate. Defect creation due to recombination decreases, and saturation occurs.

3) A reduction in device conductance after stopping a current stress is usually observed. The time dependence of the change in device conductance follows a stretched-exponential relation, $G(t) = G_{t0}exp[-(t/\tau)^{\beta}]$, where β is the dispersion factor and τ is the time constant of the degradation, both of which are found to be voltage bias and temperature dependent. It is proposed that this phenomenon may result from a change in the carrier distribution at the band tail due to current stress, i.e. by changing the coordination of dopant atoms.

4) On further increasing the current stress, large numbers of energetic (hot) electrons are generated within both the barrier and the bulk. These hot electrons may cause direct Si-H bond breaking and create defect structures along the transport path. An eventual "forming" of the device results when further stressing links these defect structures into a chain-like filamentary path. Typically, the forming current is of the order of a few tens of micro-amperes. The saturation value of V_{mea} just before forming is in the range $10-12V$, very close to the forming voltage $(12 - 14V)$ in voltage forming. The device resistance drops from several hundred megohms to a few kilohms.

5) Generally, the electrical properties of current-formed devices are very similar to those formed by a single voltage pulse. They have a I-V characteristic with a conduction activation energy (a few or few tens of milli-electron volts over the temperature range $150 - 300K$). The ERASE/WRITE current waveform responds almost instantaneously to the applied voltage signal, indicating a high switching speed. Polarity dependent switching is usually observed. In addition, the device resistance changes continuously from its ON to OFF-state, or OFF to ON-state over a voltage range of $\sim 1V$ (ERASE) or $0.2 - 0.3V$ (WRITE).

6) A temperature-induced metal-non metal (MNM) transition was observed in some current-formed devices. The dc resistance of such devices undergoes a continuous change in the range of $60 - 100K$, from semiconductor-like behaviour to metallic, as temperature increases. The ac conductivity, measured over a frequency range of $1Hz - 3.1 \times 10^7 Hz$, shows an anomalous change as temperature is varied over the MNM transition. AC characteristics were modelled using multi-component RC and RL equivalent circuits below and above the MNM transition region respectively. It is found that the capacitance increases markedly when the temperature approaches the MNM transition from the semiconductor side. Near the transition temperature this capacitance disappears, and the equivalent circuit requires an inductive component together with a resistance which has a positive TCR equivalent to that of the dc resistance in this temperature range. This anomalous behaviour is explained in terms of a percolation-like critical behaviour of the dielectric constant ϵ_{eff}, which diverges at the threshold p_c. The enhancement of the dielectric constant (capacitance) is due to a decrease in the separation (s) of metallic particles. When $s \rightarrow 0$, the volume fraction of the metallic particles approaches its critical value, p_c, which is interpreted to be the point when the metallic spheres make contact. Thus the device undergoes a metallic transition.

7) The electronic conduction in formed devices has been analysed using a general activated tunnelling approach. The results of this theoretical analysis are as follows:

i) The microstructure of the filament could be simulated as a metal-containing structure in which metallic particles are embedded in the a-Si:H network. The diameter of the filament could be $50\mathring{A}$ or less, and both particle size and the separation between these particles could be $\leq 10\mathring{A}$, assuming that the particles are spherical.

ii) The change in device resistance during analogue switching can be attributed to a change in the separation of metallic particles. The WRITE operation reduces the separation of particles, thus the resistance decreases from a high resistive state to a lower one. Vice versa, the device resistance increases during the ERASE operation because of enlargement of the separation.

iii) Beyond the ON-state, where the activation energy $\Delta E > k_B T$, the electron transport is via metallic particles within the filament by means of the activated tunnelling. However, near the ON-state when $\Delta E < k_B T$, electron tunnelling is not a thermally activated process, possibly due to a decreasing separation between particles.

10.3 Future work.

Although devices formed by constant current stressing exhibit very similar switching characteristics to those formed by voltage biasing, the main disadvantage of the former is its instability during subsequent switching operations. Thus further work in this area is necessary to enhance the durability of the devices formed by constant current forming. As shown in voltage forming, the quality of the memory switching is affected not only by the forming process, but also by many other factors such as device structure, thickness, pore size, and particularly the metal used as the top electrode. It would be helpful if a systematic investigation could be carried out in the areas mentioned above in the case of forming by current stressing. In addition, it would be worth trying to form with current pulse instead of constant current, so as to study the effect of pulse duration on forming and subsequent switching properties.

Another area of work is to further explore the origin of the metal-non metal transition occurring in current-formed samples, since this research is of fundamental importance in understanding the material properties of the conducting filament, which affects the switching characteristics so much. Although it is widely agreed that the filament is a medium consisting of metallic inclusions embedded in a silicon matrix of some kind, what is not clearly known is whether the metallic constituent is made of pure vanadium particles or compounds such as vanadium silicides and oxides. Another aspect of the work would be to use more powerful diagnostic tools, i.e. high resolution SEM/EDX combined with FIB (focus-ion-beam) technique, or possibly AFM (atomic force microscope), to determine more accurately both the filament structure and materials existing within the conducting filament.

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Appendix A

list of publications

The work described in this thesis has been reported in the following publications:

- J.Hu, J.Hajto, A.J.Snell, A.E.Owen, and M.J.Rose, "Capacitance Anomaly Near the Metal-Non Metal Transition in Cr-a-Si:H-V Thin Film Devices", *Phil.Mag.B*, 1996, Vol.74, No.1, 37-50.

- J.Hu, A.J.Snell, J.Hajto, A.E.Owen, and M.J.Rose, "Critical behavior of the dielectric properties near the metal-non metal transition in Cr/p+a-Si:H/V thin film devices", *J.Non − Cryst.Solids*, Vol.198-200(1996), 1217-1220.

- J.Hajto, A.J.Snell, J.Hu, A.E.Owen, M.J.Rose, and R.A.Gibson, "Metal-Semiconductor Transition in Electroformed Cr-amorphous silicon-V Thin Film Structures", *Phil.Mag.B*, 1994, Vol.69(2), 237-251.

- J.Hajto, A.J.Snell, J.Hu, A.E.Owen, M.J.Rose, and R.A.Gibson, "AC and DC Conductivity of Electroformed Amorphous Silicon Memory Structure", *J.Non − Cryst.Solids*, Vol.166, pp.821-824, (1993).

Paper submitted:

- J.Hu, A.J.Snell, J.Hajto, and A.E.Owen, "Constant current forming in Cr/p+a-Si:H/V thin film devices", accepted by the ICAMS 17, Budapest, Hungary, August, 1997., to be published soon on $J.Non-Cryst.Solids$.

Constant current forming in Cr/p^+a-Si:H/V thin film devices

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Experimental results on the constant current stressing and forming of hydrogenated amorphous silicon Cr-p^+-V thin film devices are presented. In the initial stage of electro-forming by constant current stressing, with increasing injection of charge via either increasing bias or time, the $I-V$ characteristics of devices exhibit an instability, as shown by a decrease in the reverse current. This is interpreted in terms of the creation of defects in the a-Si:H. The defect generation rate, as measured by the voltage shift ΔV at a constant reverse current in the $I-V$ curve, is found to follow a square-root time-dependent law. Eventually, with further increasing current bias, the local current density reaches a critical value I_F, and a rapid 'runaway' processes occurs, which results in an irreversible change of the initial high-resistance state into a permanent "formed" state of lower resistance.

1. INTRODUCTION

It is well known that an initial forming process is crucial for Cr/p^+hydrogenated amorphous silicon/V (Cr/p^+/V) structures to function as memory devices. Forming substantially changes the microstructure of the devices, creating a highly conducting filament [1]. Conventionally, the electro-forming of as-deposited (unswitched) devices is achieved by biassing the sample with a single voltage pulse, causing a substantial reduction in the high resistance state of the structure and diffusion of the top metal material (vanadium) into the a-Si:H layer. As an alternative, this paper reports measurements on *constant current* stressing and forming in Cr/p^+/V thin film devices. Possible mechanisms for the current stressing and forming process are also discussed.

2. EXPERIMENTAL

Samples used in this work were hydrogenated amorphous silicon Cr/p^+/V thin films deposited on oxidized crystalline silicon wafers. The p^+ a-Si:H layer was prepared by rf glow discharge decomposition of silane (SiH_4) containing $10^3-10^4 vppm$ of diborane (B_2H_6). Film thicknesses range from $700\AA-1200\AA$, with the contact area defined by a $10\mu m$ diameter pore in an insulating layer.

A HP4145A Semiconductor Parameter Analyser is used to provide the voltage/current output for forming. In the time domain mode, the instrument acts as a current source which stimulates the device, while a voltage monitor records and displays the change of voltage necessary to maintain a constant current with time. During current stressing the positive voltage is always applied to the top vanadium electrode, so that the V/p^+a-Si Schottky barrier is reverse biassed. The overall stressing/forming process is programmed and remote-controlled by a PC via and an IEEE488 interface. The HP4145A is also used to measure the DC properties of devices.

3. EXPERIMENTAL RESULTS

1) Electrical properties of unstressed devices.

Fig.1 shows a set of typical current vs. voltage characteristics for Cr/p^+/V devices (with a positive polarity applied to the V electrode) before stressing and for two current stressing levels measured after a fixed time of $250sec$. Note that the current passing through the reverse biased V/a-Si:H barrier exhibits a non-saturating characteristic with increasing voltage, and it increases almost exponentially with bias. The current-voltage characteristic is described well by the following thermionic-field emission equation [2]

$$J = J_s exp(V/E') \quad (1)$$

where J_s is the reverse saturation current, and V is the reverse bias voltage. The parameter E' is a complicated function of N_a, the acceptor density, m^*, the effective mass, and ε_s, the relative dielectric constant of the semiconductor [2,3].

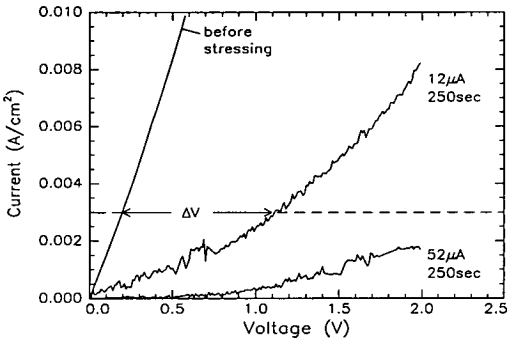

Fig. 1. I-V characteristics of a Cr-p^+-V device before and after stressing.

The thermal activation energy E_a of the current and its prefactor I_0, shown in Fig.2, also exhibit characteristics associated with thermionic-field emission. At low bias ($0.15 - 0.2V$), E_a initially increases, reaching a maximum ($\sim 0.3eV$) at about $0.2V$, then decreases to $< 0.1eV$. The prefactor I_0, which reflects the transport mechanism, shows a similar dependence. It exhibits a rapid reduction with bias at about $1V$, indicating that tunneling sets in, effectively reducing the barrier height at the contact. This causes a large

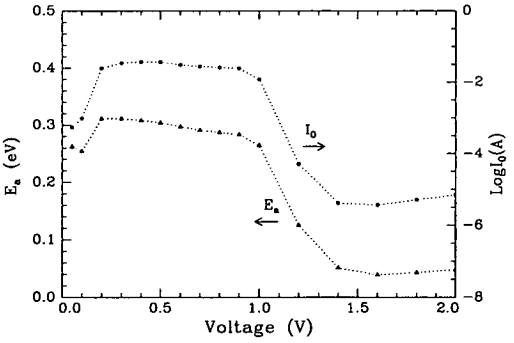

Fig. 2. Change of activation energy E_a and I_0 with voltage.

increase in the reverse current. The tunneling probably results from the high doping in the a-Si:H layer. As reported by Jackson *et al* in metal/n^+ barriers, when the doping level increases beyond $10vppm$, the effective barrier height reduces significantly, even at zero field, due to the high defect density [3].

2) Effect of current stress.

Fig.3 shows typical curves of the voltage necessary to maintain a constant current (defined as V_{mea}) as a function of the stress time for a sequence of constant current biases ($10 - 70\mu A$), at ambient temperature. At a low

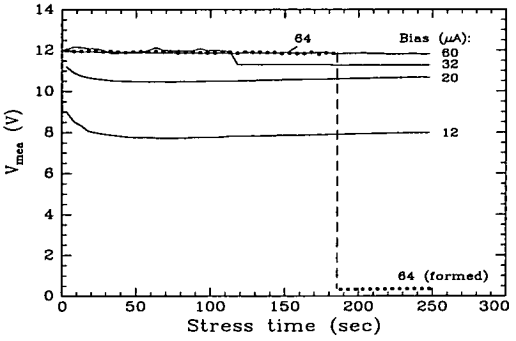

Fig. 3. Change of the voltage across the sample V_{mea} with stressing time t.

current bias V_{mea} initially decreases exponentially with time, and then becomes almost constant, possibly increasing slightly. At sufficiently long times, V_{mea} tends to saturation. This suggests that charge trapping occurs during stressing, reducing the current passing through the device, and hence V_{mea} increases to maintain a constant current. This can also be seen from Fig.1, where ΔV is the voltage shift required to maintain an arbitrary current density (about $3mA/cm^2$ in this example). The voltage shift ΔV is a function of current stress and time:

$$\Delta V = kI^{1/2}t^{\lambda} \quad (2)$$

where k is a constant and λ is approximately 0.5. Fig.4 shows the corresponding change in I-V characteristic with time, where the current stress is kept constant at $I = 10nA$. The time dependence of ΔV described by Eq.(2) is illustrated in Fig.5.

3) The forming of devices.

As seen in Fig.3, on increasing the current

bias to $64\mu A$ a critical stage is reached at which forming occurs. The device resistance drops from several hundred megohms to a few kilohms. The forming current I_F is of the order of a few tens of micro-amperes ($64\mu A$ in the case of Fig.3). It was found that the history of samples after deposition affects I_F. This may result from a change in the surface layer of devices due to oxidation of electrode. But the saturation value of V_{mea} $(10-12V)$ just before forming is always very close to the forming voltage $(12-14V)$ in voltage forming [4].

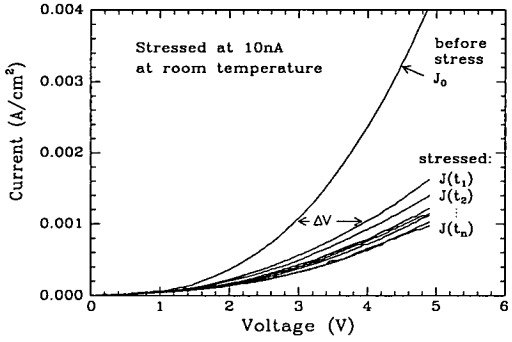

Fig. 4. Change in I-V characteristics with stress time.

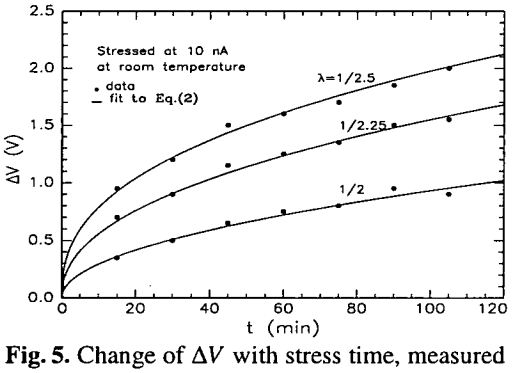

Fig. 5. Change of ΔV with stress time, measured at three different current values in I-V curves (Fig.4). The lines are fitting results by Eq.(2).

4. DISCUSSION

1) Defect generation.

The square-root kinetics of Eq.(2) are frequently observed in the defect generation process in other a-Si:H diode structures when stressed with a constant current [5,6]. This characteristic can be explained by a model based on electron-hole recombination with the assumption that the hole concentration is proportional to the current flowing into the anode [7]. The released recombination energy breaks weak Si-H bonds and the freed hydrogen atoms move to break weak Si-Si bonds, leading to the generation of additional deep gap states. The newly-created defects in turn reduce the life time of carriers, and thus the recombination rate. Further defect creation due to recombination decreases, and saturation occurs.

A similar mechanism could be applicable to the a-Si:H Cr-p^+-V devices where a sublinear time dependence is also observed. The band diagram for a reverse-biassed a-Si:H Cr-p^+-V diode is shown schematically in Fig.6, with

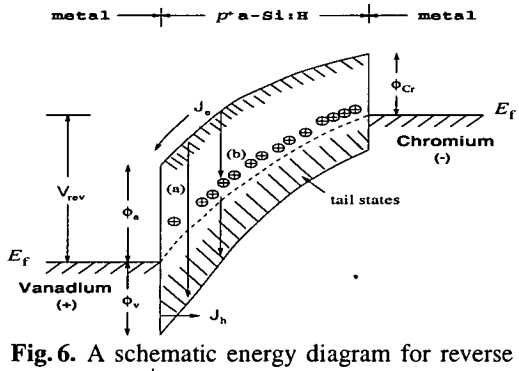

Fig. 6. A schematic energy diagram for reverse biassed Cr-p^+a-Si:H-V structures. (a) band-tail electron-hole recombination; (b) recombination via O defects near E_F.

positive polarity applied to the top vanadium electrode. During stressing, electron-hole recombination occurs between electrons injected from the cathode (Cr electrode) and trapped holes at the valence band edge (indicated in the figure as process (a)). Another recombination path is via those charged states O near E_F (process (b)) which also act as dominant trapping centers. A O state (Si_3^+) is paired with ionized fourfold-coordinated dopants (B_4^-). The B_4^--Si_3^+ pair is equilibrated with electrically inactive threefold-coordinated structures (B_3^0) and neutral dangling bonds (Si_4^0), i.e.

$$B_3^0 + Si_4^0 \Leftrightarrow B_4^- + Si_3^+ \qquad (3)$$

Although recombination via path (b) is a two-

stage process, the recombination rate could be very high because of the high tail-state density ($\sim 10^{18} cm^{-3}$ in the present case of $10^3 \sim 10^4 vppm$ doping) [8]. Moreover, the quasi-Fermi level is $\sim 0.2eV$ from the valence band edge due to high doping [9]. The O states are located at the band tail, and trapped electrons thus have a high probability of recombining with trapped holes via tunneling. The energy released by this recombination creates more Si_4^0 states, and the concentration of Si_3^+ due to electron trapping decreases. As a result, more B_4^- states convert into B_3^0. The subsequent saturation in ΔV results from either a reduction in carrier lifetime due to the appearance of more Si_4^0, or the filling of Si_3^+ (O) states. Both reduce the states available for recombination and trapping, and reduce the defect-creation rate.

2) Possible forming mechanism.

As pointed out above the reason for defect creation is the breaking of weak Si-Si and Si-H bonds, with the mediation of hydrogen. Electron-hole recombination is a self-limiting process and hence on increasing the bias, the recombination rate will decrease gradually due to the lower capture cross section and/or lower carrier densities. Note that the average field across the specimen increases with bias, as measured by V_{mea}. Under high fields, hot electron effect may occur, resulting in direct dangling bond formation. In addition, hot electrons that drop into the Fermi level of the metal at the anode release a substantial energy, which leads to a further breaking of Si-Si and Si-H bonds. When the current bias exceeds its critical value those defects in the bulk and at the interface could link in a chain and thus form a filamentary path. The device current then increases rapidly. Defect formation is particularly severe in the interface near the anode, as most weak bonds are located in the interfacial region and also the highest field strength exists there. A similar mechanism was proposed to account for the breakdown in SiOx dielectric films [10,11].

5. CONCLUSION

Current transport in an unstressed reverse-biassed Cr/p^+a-Si:H/V devices is controlled mainly by thermionic-field emission of carriers over the V/a-Si:H barrier. When the device is stressed at a constant current bias, a time-dependent voltage shift ΔV in its I-V characteristic is observed, which usually varies as the square root of time. This is explained qualitatively by electron-hole recombination at the interface and in the a-Si:H bulk. On further increasing the current stress, large numbers of energetic (hot) electrons are generated within both the barrier and the bulk. These hot electrons may cause direct Si-H bond breaking and create defect structures along the transport path. The eventual "forming" of the device results when further stressing links these defect structures into a chain-like filamentary path.

6. ACKNOWLEDGMENT

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Critical behavior of the dielectric properties near the metal-non metal transition in Cr/p^+a-Si:H/V thin film devices

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The ac conductivity data for Cr/p^+hydrogenated amorphous silicon/V thin film devices, measured over a frequency range of $1Hz$~$30MHz$ and a temperature range 13~$300K$, has been modelled using multi-component RC and RL equivalent circuits below and above the metal-non metal (MNM) transition region respectively. The capacitance (dielectric constant) anomaly near the metal non-metal transition is explained in terms of a percolation-like critical behaviour of the dielectric constant ε_{eff}, which diverges at the threshold of the volume fraction of the metallic particles, P_c.

1. INTRODUCTION

It has been observed recently that the electrical properties of Cr/p^+hydrogenated amorphous silicon(a-Si:H)/V thin film analogue memory structures change from a semiconducting behaviour to a metallic behaviour as a result of systematically changing the temperature for a fixed memory state [1]. The ac characteristics also show significant changes. The capacitance, obtained by fitting the experimental data to an equivalent circuit, shows an abnormal increase, which cannot be explained by a simple geometric model based on a parallel plate capacitor because the area of the capacitor would need to be larger than the area of the device. In this paper, we further analyse the anomaly of the filament capacitance.

2. DEVICE STRUCTURE

Samples used in this work were amorphous silicon $Cr - p^+ - V$ sandwich structures configured as shown in Fig.1. The p^+-amorphous silicon layer, with thickness of $1000\AA$ is prepared by rf-glow-discharge decomposition of silane (SiH_4) containing typically 10^4 ppm by volume of diborane (B_2H_6). The initial forming for as-deposited (unswitched) devices was achieved by biassing the sample with a current source. Forming substantially changes the original uniform amorphous silicon structure. Device resistance decreases from 10^6~10^9 to 10^3~$10^4\Omega$. A highly conducting filament is created inside the device. DC and ac behaviour were measured using a HP 4145A Semiconductor parameter Analyser (dc) and a Schlumberger 1260 impedance analyser (ac) over a frequency range from 1 Hz to 32 MHz.

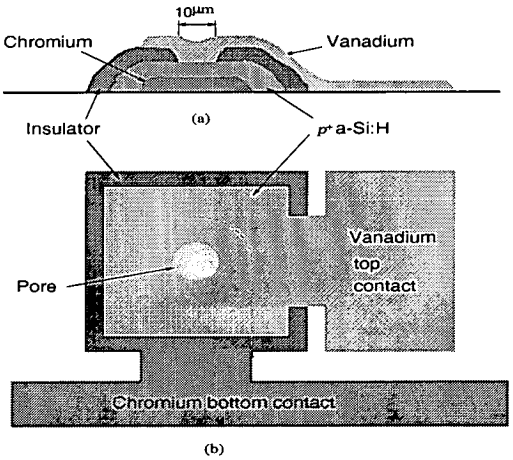

Fig. 1. The Structure of p^+ amorphous silicon memory device.

The measured ac conductivity data are simulated by a complex non-linear least square (CNLS) fit procedure [2]. In this procedure a model circuit is first obtained by analysing successive region of the measured frequency response, and circuit parameters are then optimised by the total non-linear least square fit program, which leads to an optimization of the fit for experimental data.

3. EXPERIMENTAL RESULTS

Figure 2 shows the dc resistances as a function of temperature for three typical samples. In the temperature region from $13K$ to about 60K the resistance of all samples decreases with increasing temperature indicating that the conduction process is of a semiconductor type. The activation energy (ΔE) can be

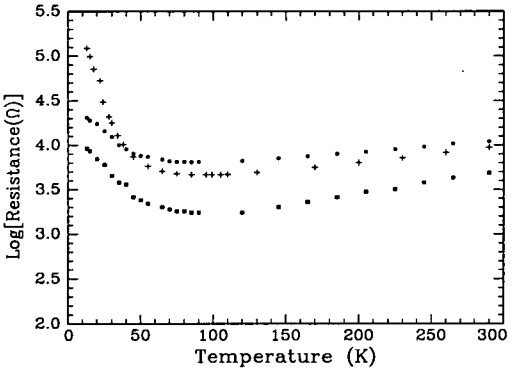

Fig. 2. DC resistance vs. temperature.

calculated from the Arrhenius plot as 1.18~6.29meV (20~60K) and 0.22~2.49meV (13~20K), respectively. Between 60~100K there is a region where the resistance undergoes a continuous change. It first decreases slightly to a minimum value and then increases almost linearly with increasing temperature indicating a metallic type conduction. The transition temperature, T_{tr} at which the minimum resistance occurs is not same for different samples, but found to be within a range from 70K to 100K.

Above T_{tr} the resistances increase slightly with the increasing temperature and show metallic behaviour. The temperature coefficient of resistance, TCR (defined as $(1/R_0)(dR/dT)$), is in the range $3\sim5\times10^{-3}K^{-1}$, which is fairly close to the corresponding values for vanadium in the temperature range 100~300K ($4.513\times10^{-3}K^{-1}$) [3]. This indicates that the metallic conduction occurring above T_{tr} is closely associated with the presence of vanadium, which is introduced into the a-Si:H material during the forming process.

The differences occurring in ΔE, T_r, and positive TCR among these samples probably result from electro-forming process, which at the moment cannot be controlled precisely. The diffusion of top vanadium will lead to slightly different microstructure of the filament which could affect macro-properties of devices like ΔE, T_r, and TCR.

Fig.3 shows the ac conductance $\sigma(\omega)$ as a function of frequency at different temperatures, where $\omega = 2\pi f$ is angular frequency. In the frequency range $10^3\sim10^4Hz$, $\sigma(\omega)$ shows distinctive changes. The ac behaviour is capacitive at temperatures lower or equal to 55K. However, it changes rather drastically when temperature is over 55K. The capacitive relaxation disappears, and the ac conductance $\sigma(\omega)$ decreases with increasing frequency,

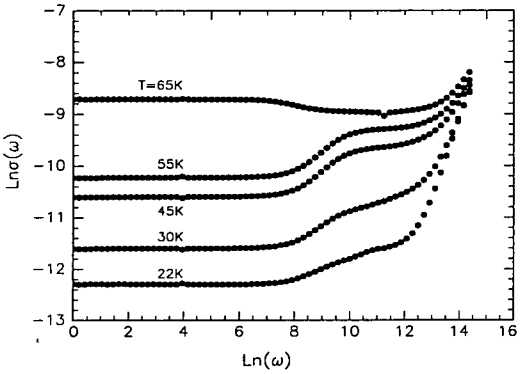

Fig. 3. AC conductance vs. frequency at different temperature.

indicating the onset of an inductive effect.

4. ANALYSIS AND DISCUSSION

1) Equivalent circuits and filament structure

The above ac characteristics have been analysed by the CNLS-fit procedure mentioned before, and modelled by the equivalent circuits illustrated in Fig.4(a) and (b) respectively. The physical meaning of the circuit parameters is described in terms of the microstructure of the filament shown Fig.4(c). R_s is a contact resistance between the electrodes and the filament, while C_∞ probably comes from the insulating media surrounding the filament. R_1 could be associated with the bulk resistance of the metallic particles embedded the in a-Si:H, while R is the 'gap' resistance between metallic particles and C the capacitance associated with R. At higher temperatures, i.e. $T > T_{tr}$, the filament becomes metallic. L probably arises from the interaction among various metal conduction paths.

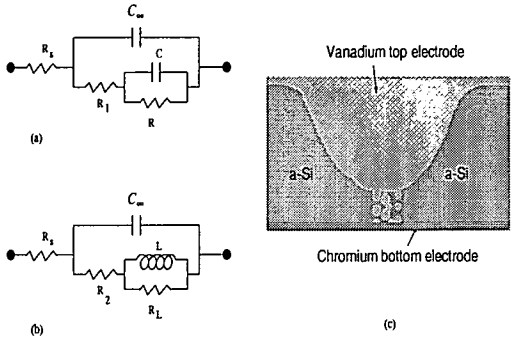

Fig. 4. Equivalent circuits for (a) $T \leq 55K$, (b) $T \geq 65K$, and (c) supposed microstructure of filament.

Figure 5 shows the temperature dependence of C and C_∞ in the range of 13~300K. These capacitance values are obtained from the CNLS-fit of experimental data at different temperature, modelled with the equivalent circuit shown in Fig.4(a) and (b). It is observed that C, associated with R, shows an extraordinary increase from $170pF$ at $13K$ to $2489pF$ at $55K$ as the temperature approaches the MNM transition from the semiconductor side, and then disappears when temperature is over $65K$.

2) Effective dielectric constant of the filament

The effective dielectric constant $\varepsilon_{eff}(\omega)$, can be deduced from the measured ac characteristics, that is, $\varepsilon'(\omega) \equiv \mathrm{Im}[Y(\omega)/\omega C_0]$, where the admittance $Y(\omega)$ is for the equivalent circuit in $T \leq 55K$ (Fig.4(a)). Therefore, the effective static dielectric constant, found when $\omega = 0$, is:

$$\varepsilon_{eff} = \varepsilon'(0) = \frac{C_\infty}{C_0} + \frac{C}{C_0}\frac{R^2}{(R_1+R)^2} \qquad (1)$$

where C_0 is the capacitance without the metallic particles. In equation (1) we have ignored the contact resistance R_s, since it has a negligible effect on the main characteristics.

Equation (1) directly relates ε_{eff} with capacitance C. Substituting the data for C, C_∞, R, and R_1 in the equivalent circuit into equation (1), we obtain the change of ε_{eff} against temperature, which changes from about 836 at $13K$ to nearly 13612 at $55K$, or ε_{eff} increases by as much as 16 times. These results show that the anomalous change in C is associated with the change in ε_{eff} of the filament material.

3) About the enhancement of ε_{eff}

The anomalous increase in dc dielectric constant near a metal-non metal transition has been widely observed in various materials [4-8]. In the

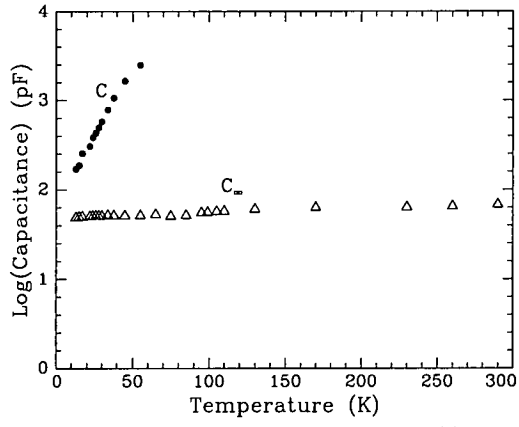

Fig. 5. Change of capacitances C and C_∞ with temperature. The capacitances are obtained from the CNLS-fit of data at different temperature.

present case of a temperature-induced MNM transition, there is the possibility that the temperature may affect the distribution of metallic particles inside the conducting filament, or more specifically, inside the remaining a-Si:H area, so that ε_{eff} shows an anomalous change. In the following, we apply percolation theory to describe ε_{eff}. In this way, we can correlate the change in ε_{eff} with the microstructure of the filament.

According to percolation theory, the effective static dielectric constant can be expressed by the following formula [9,10]:

$$\varepsilon_{eff} \sim \varepsilon_h \left| \frac{p - p_c}{p_c} \right|^{-q} \qquad (2)$$

where q (-1.3) is the critical exponent for a two-dimension heterogenous conductor-dielectric binary composite, ε_h is the dielectric constant of the host material, and p and p_c are volume fraction of the particles and the threshold respectively. Assuming that the remaining a-Si:H layer (see Fig.4(c)) has a cylindrical shape, and the embedded particles are spheres with the radius r, then ε_{eff} can be related to the spacing s between particles and their radius r:

$$\varepsilon_{eff} \sim \varepsilon_h \left| \frac{kr^3/(s+r)^3 - p_c}{p_c} \right|^{-q} \qquad (3)$$

where k is a constant. The dimension of the embedded particles inside the a-Si:H layer can be estimated from the activation energy. Electron transport in a-Si:H containing metallic particles can be assumed to be an activated tunnelling process. The activation energy ΔE is related to the particle radius r by: $\Delta E = e^2/\varepsilon_r \varepsilon_0 r$ [11]. Using experimental data of $\varepsilon_r = \varepsilon_{eff} \sim 1500$ and $\Delta E = 1.8\text{-}6.2meV$, the radius of particles is in the range of $1.6\text{-}5.3\dot{A}$.

The critical volume filling factor is treated as an adjustable parameter. The relative change of the effective dielectric constant has almost same magnitude as that shown in experiments, i.e. for the particles with radius of $2\dot{A}$, $\varepsilon_{eff}/\varepsilon_h$ increases from ~1.03 to 18.6 when s decreases from ~$5\dot{A}$ to ~$0.07\dot{A}$, compared to the increase of $\varepsilon_{eff}/\varepsilon_h$ from 1 to 16 experimentally. Therefore, the enhancement of C can be well explained in terms of a percolation-like critical behaviour of the dielectric constant, which diverges at the threshold p_c.

5. CONCLUSION

The anomalous behaviour of filament capacitance (dielectric constant) has been explained in terms of a percolation-like critical behaviour of the dielectric constant ε_{eff}, which diverges at the threshold p_c. Analysis shows that the structure of formed $Cr/p^+a-Si:H/V$ devices could be modelled as an extremely thin heterogeneous medium composed of metallic particles and insulator host (e.g.a-Si:H), together with a metallic inclusion. These metallic particles originate from the diffusion of the top vanadium electrode during the forming process. The enhancement of the dielectric constant (capacitance) is due to the decrease of the separation (s) between these metallic particles. When $s \rightarrow 0$, the volume fraction of the metallic particles approaches its critical value, p_c, which is interpreted to be the point when the metallic spheres make contact. Thus the device undergoes a metallic transition.

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Capacitance Anomaly Near the Metal-Non-Metal Transition in Cr-a-Si:H-V Thin Film Devices

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ABSTRACT

We present experimental results that show a metal-non-metal (MNM) transition occurring in hydrogenated amorphous silicon (a-Si:H) analogue memory devices as a function of temperature. The DC resistance of the devices undergoes a continuous change in the range of $65\sim100°K$, from a semiconductor-like behaviour to a metallic one, as temperature increases. The AC conductivity, measured over a frequency range of $1Hz\sim3.1\times10^7Hz$, shows an anomalous change as temperature is varied over the MNM transition. AC characteristics were modelled using multi-component RC and RL equivalent circuits below and above the MNM transition region respectively. It is found that the capacitance increases markedly when the temperature approaches the MNM transition from the semiconductor side. Near the transition temperature this capacitance disappears, and the equivalent circuit now requires an inductive component together with a resistance which has a positive TCR equivalent to that of the dc resistance in this temperature range. This anomalous behaviour is explained in terms of a percolation-like critical behaviour of the dielectric constant ε_{eff}, which diverges at the threshold p_c.

1. INTRODUCTION

Electro-formed Cr/p^+ hydrogenated amorphous silicon/V thin film structures exhibit extremely fast, non-volatile, and polarity dependent memory switching properties. These memories could potentially be used as a non-volatile storage of analogue synaptic weights and integrated with conventional *CMOS* circuitry (Holmes *et al*, 1993).

It has been shown that a highly conducting filament is created after electro-forming of the analogue memory devices, which is the result of diffusion of top vanadium atoms into the a-Si:H network (LeComber *et al*, 1985). Additional experimental results suggest that the filament contains metallic particles embedded in an insulating network (Hajto *et al*, 1991; Jafar and Haneman, 1994a). The electrical properties of the Cr/p^+a-Si:H/V thin film structures rely crucially on the conducting filament. It is difficult to observe directly the microstructure of this conducting filament due to its extremely small size. However a number of experimental results indicate that the structure of the formed a-Si:H memories consist of two parts. One is the metal-containing region resulting from the diffusion of the top metal. The other is the remaining a-Si:H matrix of relatively high resistance. It has been shown that the memory mechanism could partly be explained for such a structure by assuming that the metallic inclusion is positively charged (Jafar and Haneman, 1994b).

Under an applied electric field these charged particles will move slightly. This is equivalent to the length of the remaining a-Si:H changing by an amount Δl, and thus the a-Si:H resistance changes by ΔR. A reasonable relationship between ΔR and Δl can be obtained by combining such a microstructure of the filament with other observed terms, i.e. the OFF to ON transition time. In addition, the quantization of the device resistances observed in low temperatures could also be qualitatively explained by assuming that the tip of the metallic inclusion is so close to the bottom electrode that the contact area may contain only one single atom or small number of atoms. This forms an atomic point contact system where the resistance would be $h/2e^2$ (associated with a single atom) or $h/2ie^2$ where i is an integer (associated with several atoms) (Hajto *et al*,1991).

It has been observed recently that the electrical properties of the Cr/p^+a-Si:H/V thin film analogue memory structures change from a semiconducting behaviour to a metallic behaviour (metal-non-metal transition, MNM transition) as a result of a systematic decrease of the resistance of the analogue memory state or a change of the temperature for a fixed memory state (Hajto *et al*, 1994). In the latter case the AC characteristics also show significant changes.

The capacitance, obtained by fitting the experimental data to an equivalent circuit, shows an abnormal increase when the temperature approaches the MNM transition from the semiconductor side, which cannot be explained by a simple geometric model based on a parallel plate capacitor because the area of the capacitor would need to be larger than the area of the device.

In this paper, we will further analyse the filament capacitance, and show that the increase in capacitance in fact reflects the anomalous increase of the effective dielectric constant of the filament material. Near the MNM transition, the effective dielectric constant exhibits a percolation-like critical behaviour.

2. STRUCTURE AND PREPARATION OF DEVICES

Samples used in this work were amorphous silicon $Cr - p^+ - V$ sandwich structures deposited on Si wafers, which are configured as shown in Fig.1. The p^+-amorphous silicon layer, with thickness of $1000\dot{A}$ is prepared by rf-glow-discharge decomposition of silane (SiH_4) containing typically 10^4 ppm by volume of diborane (B_2H_6), with the contact area defined by a 10-μm-diam pore in an insulating layer. The top (V) and bottom (Cr) metal electrodes are prepared by vacuum evaporation. The initial forming for as-deposited (unswitched) devices was achieved by biassing the sample with a constant current. The forming current density varies from 0.06 to $0.38 A/cm^2$, and the time required to form the sample varies from 5 to 45 minutes, depending on current level. Forming substantially changes the originally uniform amorphous silicon structure. A highly conducting filament is created inside the device. Device resistance decreases from 10^6~10^9 to 10^3~$10^4\Omega$. DC and AC behaviour have been measured using a HP 4145A Semiconductor parameter Analyser (DC) and a Schlumberger 1260 impedance analyser (AC) over a frequency range from 1 Hz to 32 MHz, over the temperature range from 13K to 300K. The Schlumberger 1260 impedance analyser has a nulling facility to compensate for stray capacitance during impedance measurements. Therefore, the stray capacitance could be effectively excluded. For the measurement of DC and AC characteristics over a wide temperature range, a Displex Closed-Cycle Refrigeration System was used. Cryogenic temperatures as low as $10K$ can be achieved in this system.

The measured AC impedance data have been simulated by a complex non-linear least square (CNLS) fit procedure (Boukamp, 1986). In this procedure a model circuit is first

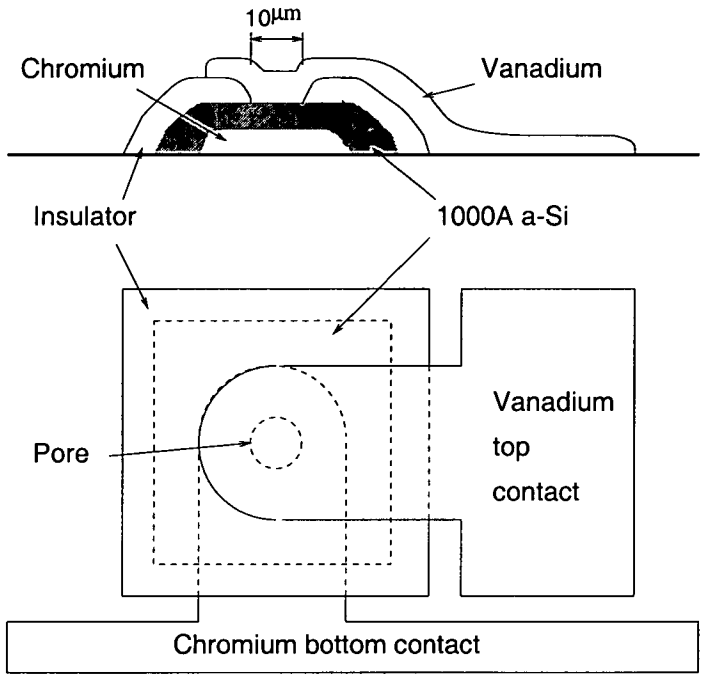

Fig. 1. The structure of p^+amorphous silicon memory devices.

obtained by analysing successive regions of the measured frequency response, and circuit parameters are then optimised by the total non-linear least square fit program, which leads to an optimization of the fit for the experimental data.

3. EXPERIMENTAL RESULTS

1) DC Characteristics

Fig.2 shows DC resistance as a function of temperature for three samples A, B, and C, which were electro-formed at room temperature using the forming conditions described previously. The room-temperature DC resistance values of samples A, B, and C are $1.1\times10^4\Omega$, 9468Ω, and 4850Ω, respectively. These variations are probably caused by slight differences in the structure of the filament formed in the devices. In the temperature region from $13K$ to about 60K the resistance of all samples decreases with increasing temperature, indicating a semiconductor type conduction process. Between $60\sim100K$ there is a region where the resistance undergoes a continuous change. It first decreases slightly to a minimum value and then increases almost linearly with increasing temperature indicating a metallic type conduction. The transition temperature, T_{tr} at which the minimum resistance occurs is not the same for different samples, but is found to be within a range from $70K$ to $100K$. Fig.3 shows the Arrhenius plots of the these samples. On the semiconductor side of the MNM transition (below $60K$), it can be clearly seen that there are two temperature regions where the conduction can be characterised by two activation energies. The conduction in this case can be described by:

$$\sigma = \sigma_1 exp(-\frac{\Delta E_1}{kT}) + \sigma_2 exp(-\frac{\Delta E_2}{kT}) \qquad (1)$$

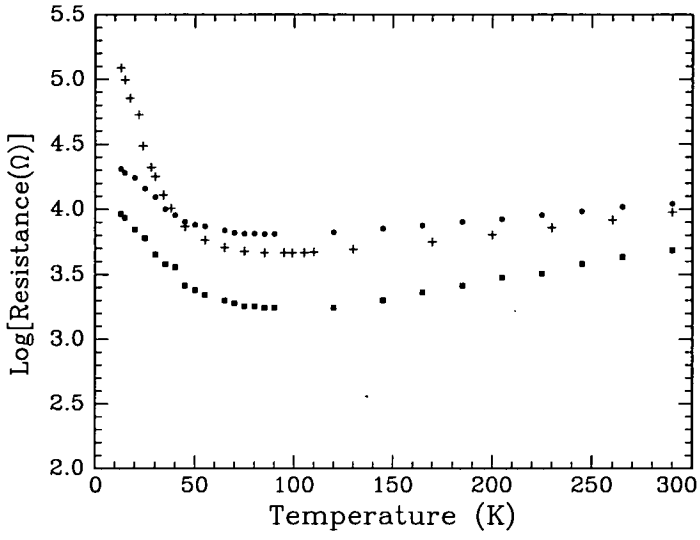

Fig. 2. DC resistance vs. temperature.

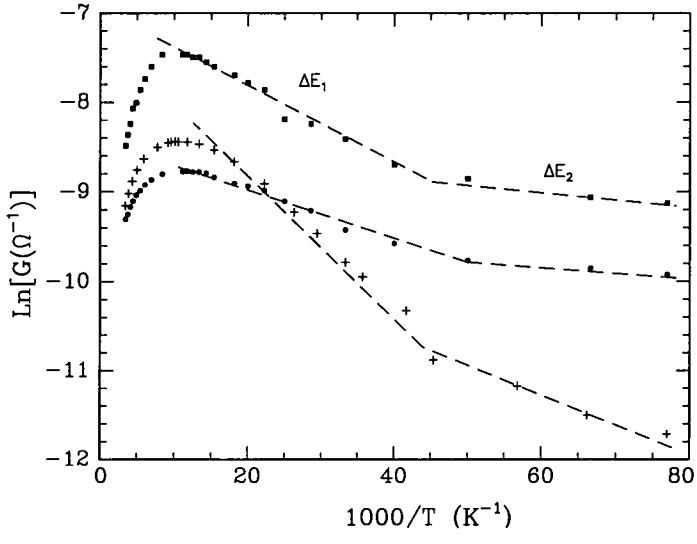

Fig. 3. Arrhenius plot of DC conductance.

By fitting the data to equation (1), we obtain $\Delta E_1 = 1.18\sim6.29meV$ and $\Delta E_2 = 0.22\sim2.49meV$, respectively.

Above T_{tr} the resistances increase slightly with increasing temperature and show metallic behaviour. The resistance *vs* temperature curve can be best described by the following empirical form:

$$R(T) = A + B(T - T_{tr}) + C(T - T_{tr})^2 \quad (2)$$

where A, B, C are constants depending on the sample. The temperature coefficient of the resistance, TCR, defined by $\alpha_0 = (1/R_0)dR/dT$ (R_0 is the resistance at $273K$), is in the range of $3\sim5\times10^{-3}K^{-1}$, which is fairly close to the corresponding values for vanadium in temperature range of $100\sim300K$ ($4.513\times10^{-3}K^{-1}$) (Lide, 1992). This indicates that the metallic conduction occurring above T_{tr} is closely associated with the presence of vanadium, which is introduced into the a-Si:H material during the forming process.

The differences occurring in ΔE, T_{tr}, and the positive TCR among these samples probably arise from the nature of the electro-forming process. Although the samples under test originated from a single batch, and thus have the same doping level and p^+ layer thickness, the current densities required to form the samples show some variation. Thus the forming process, driven by different current densities, could lead to slightly different microstructures in the filament, e.g. a different particle size distribution for the embedded vanadium particles in the a-Si:H matrix (see Fig.8(c)), which could affect the macro-properties of the devices such as ΔE, T_{tr}, and the TCR.

2) AC Characteristics

Figure 4 shows the AC conductance $\sigma(\omega)$ as a function of frequency at different temperatures, where $\omega = 2\pi f$ is the angular frequency. In the frequency range $10^3\sim10^4Hz$,

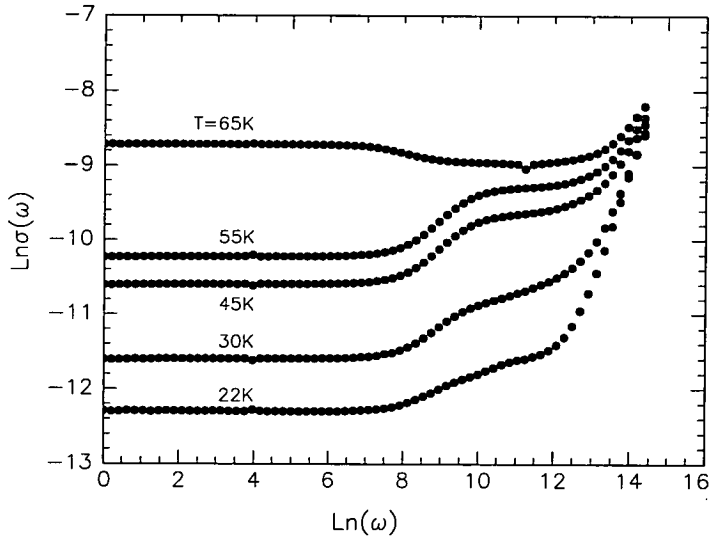

Fig. 4. AC conductance vs. frequency at different temperatures.

$\sigma(\omega)$ shows distinctive changes. The AC behaviour is capacitive at temperatures lower or equal to 55K. However, it changes rather drastically when the temperature is over $55K$. The capacitive relaxation disappears, and the AC conductance $\sigma(\omega)$ decreases with increasing frequency, indicating the onset of an inductive effect. The above transition behaviour is more clearly shown in the form of a Cole-Cole plot as illustrated in Fig.5, where the imaginary part of impedance -Im(Z) is plotted against the real part of impedance Re(Z) at temperatures $T = 55K$ and $T = 65K$. The larger relaxation in the lower frequency range completely disappears at T=65K and a new semicircle is formed (associated with an inductive effect in the negative quadrant). It should be pointed out that the MNM transition for this sample actually occurs at $T_{tr}\sim95K$ according to its DC behaviour. The AC conductance, however,

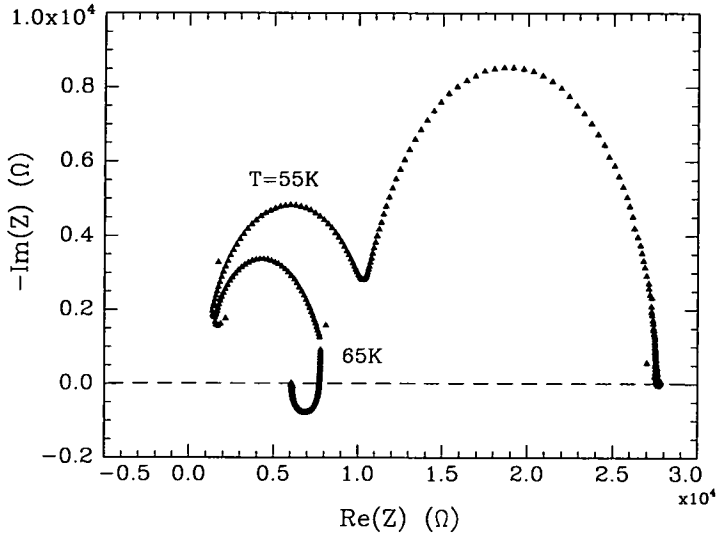

Fig. 5. Cole-Cole plot of impedance data.

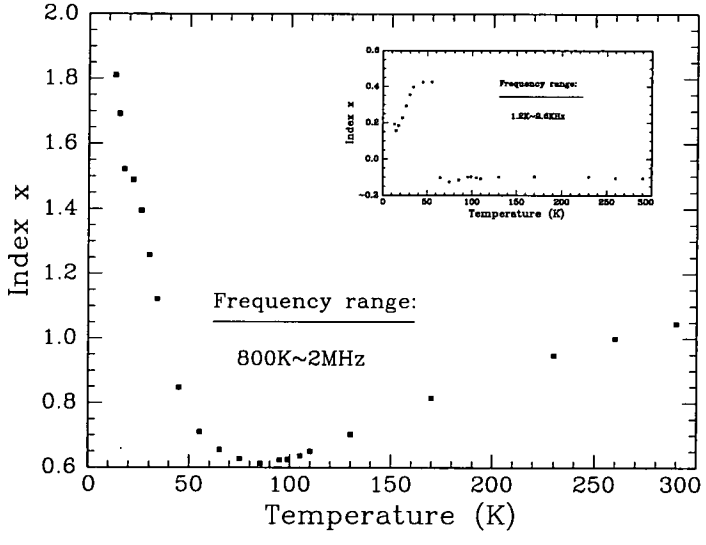

Fig. 6. Change of the exponential index x with temperature in high frequency region $800k\sim2MHz$. The inserted figure describes the lower frequency region (from 10^3 to $10^4 Hz$). Index x is defined as the slope of curve $Ln\sigma$ vs. $Ln\omega$ in corresponding frequency regions. Index values are obtained from the fitting of measured frequency responses in Fig.4 to Eq.(3).

shows an apparently broader transition starting from $65K$. This might be due to the fact that near the transition the electron transport occurs via both metallic and insulating media. DC measurement mainly detects the 'gap' resistance, while in the case of AC measurement the

AC voltage probably shorts the gap at a certain frequency so that the metallic behaviour can be observed at a lower temperature.

From Fig.4 we also can see that the frequency dependence of $\sigma(\omega)$ in both high ($800k$~$1MHz$) and low (10^3~$10^4 Hz$) frequency regions exhibit the following power law:

$$\sigma(\omega) \propto \omega^x \tag{3}$$

The exponent x is defined as the slope of the curve $Ln\sigma$ vs. $Ln\omega$ in these two frequency regions. By fitting Eq.(3) to the measured frequency response at different temperature over the range of 13~$300K$, we find that index x changes with temperature systematically in the high frequency region, as shown in Fig.6. x decreases first from near 1.9 at $13K$ to a minimum value of 0.61 and then rises again to ~1 at room temperature. In the lower frequency range (see inserted figure), x increases from 0.156 at $15K$ to 0.426 at $55K$. However, it changes sign to almost a constant negative value, i.e.~ – 0.10 above $60K$.

It is found that the dielectric constant $\varepsilon(\omega)$ in the corresponding frequency regions also obeys a power-law behaviour:

$$\varepsilon(\omega) \propto \omega^{-y} \tag{4}$$

The temperature dependence of $\varepsilon(\omega)$ in both the low and high frequency ranges are shown in Fig.7(a) and (b) respectively. The exponent y in low frequencies shows a systematic increase

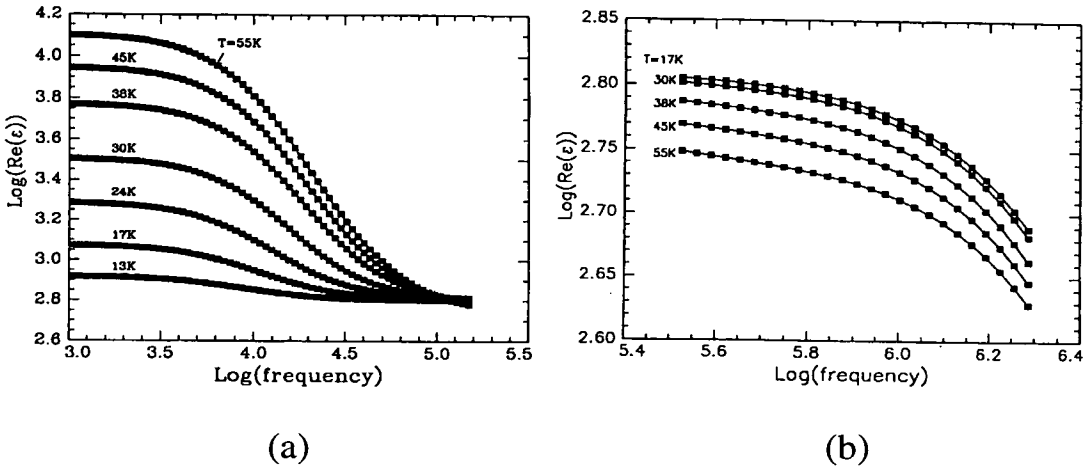

Fig. 7. Frequency dependence of $\varepsilon(\omega)$: (a) at low frequency; (b) at high frequency.

with temperature, from 0.120 to 1.18, while at high frequencies, y is almost unchanged (0.350±0.015).

It is interesting to note that near the transition temperature T_{tr} the sum of x (conductance exponent) and y (dielectric constant exponent) for high frequency regions is close to unity. For example, $x(T = 65\text{~}100K) = 0.61$ and $y(T = 55K) = 0.35$, respectively, which makes $x + y = 0.96$; while in low frequency region, although $y < 0$ when $T > 60K$, $x(T = 65\text{~}100K) = -0.10$ and $y(T = 55K) = 1.18$, thus $x + y = 1.08$. This suggests that the metal-non metal transition in the present case could be of percolation-like type, since percolation theory predicts that near the percolation threshold p_c $\sigma(\omega, p)$ and $\varepsilon(\omega, p)$ of a

random mixture should obey the power-law behaviour, and the exponents x (for $\sigma(\omega, p_c)$) y (for $\varepsilon(\omega, p_c)$) should satisfy $x + y = 1$ (Bergman and Imry, 1977).

4. ANALYSIS AND DISCUSSIONS

1) Equivalent circuits and filament structure

By using a complex non-linear least square (CNLS) fitting procedure, AC characteristics can be modelled by the equivalent circuits illustrated in Fig.8(a) and (b) respectively. The physical meaning of these circuit parameters is described in terms of the microstructure of the filament shown in Fig.8(c). R_s is a contact resistance between electrodes and the filament, while C^* probably comes from the insulating media surrounding the filament. R_1 could be associated with the bulk resistance of the metallic particles embedded in a-Si:H, while R is the 'gap' resistance between metallic particles and C the capacitance associated with R. At higher temperatures, i.e. $T > T_{tr}$, the filament becomes metallic. L probably arises from the interaction among various metal conduction paths.

Figure 9 shows the temperature dependence of C and C^* in the range of 13~300K. These capacitance values are obtained from the CNLS-fit of experimental data at different temperature, modelled with the equivalent circuit shown in Fig.8(a) and (b) respectively. It is observed that C^* is almost unchanged in the whole temperature range; however, C, associated with R, shows an extraordinary increase from 170pF at 13K to 2489pF at 55K as the temperature approaches the MNM transition from the semiconductor side, and then disappears when the temperature is over 65K.

2) Effective dielectric constant of the filament

The effective dielectric constant $\varepsilon_{eff}(\omega)$ can be deduced from the measured AC characteristics, that is, $\varepsilon'(\omega) \equiv \mathrm{Im}[Y(\omega)/\omega C_0]$. From Fig.8(a) the admittance $Y(\omega)$ for the

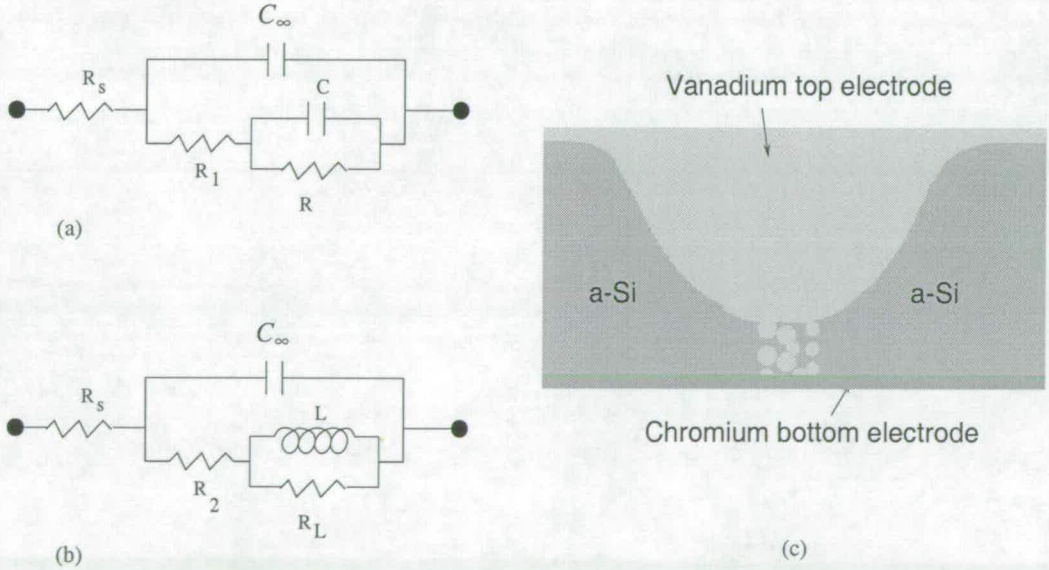

Fig. 8. Equivalent circuits for (a) $T \leq 55K$, (b) $T \geq 65K$, and (c) supposed microstructure of filament.

equivalent circuit in $T \leq 55K$ is given by

$$Y(\omega) = \frac{R_1 + R + R_1(\omega CR)^2}{(R_1 + R)^2 + (\omega CRR_1)^2} + j[\omega C^* + \frac{\omega CR^2}{(R_1 + R)^2 + (\omega CRR_1)^2}] \quad (5)$$

where C_0 is the capacitance without the metallic particles. In equation (5) we have ignored the serial resistance R_s, since it has a negligible effect on the main characteristics. When $\omega = 0$ the effective static dielectric constant thus is found to be

$$\varepsilon_{eff} = \varepsilon'(0) = \frac{C^*}{C_0} + \frac{C}{C_0}\frac{R^2}{(R_1 + R)^2} \quad (6)$$

The equation (6) directly relates ε_{eff} to the capacitance C. Substituting the data for C, C^*, R, and R_1 from the equivalent circuit into equation (6), we obtain the change of ε_{eff} against temperature, which is shown in Fig.10. It is seen that ε_{eff} changes from about 836 at $13K$ to nearly 13612 at $55K$, or ε_{eff} increases by a factor as high as 16. These results suggest that the anomalous change in C is associated with the change in ε_{eff} of the filament material. It should be also noted that a large value of ε_{eff} (836 at $13K$) provides experimental evidence for the presence of metallic particles in the amorphous silicon matrix.

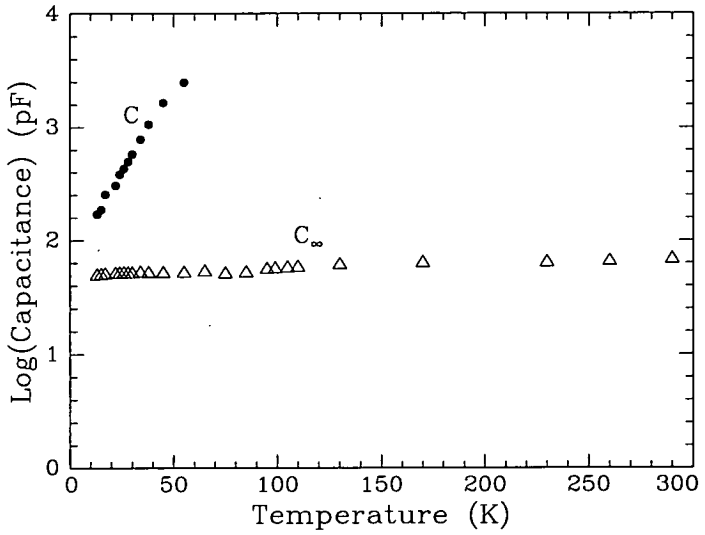

Fig. 9. C and C^* vs. temperature. The capacitances are obtained from the CNLS-fit of data at different temperature.

3) About the enhancement of ε_{eff}

The anomalous increase in DC dielectric constant near a metal-non-metal transition has been widely observed in various materials, including heavily doped semiconductors (Castner *et al*, 1975), metallic clusters (Grannan *et al.*, 1981; Chen and Johnson, 1986), metallic granular thin films (Laibowitz and Gefen, 1984), powder mixtures (Laugier *et al.*, 1986), porous ceramics (Brouers and Ramsamugh, 1986,1988), *etc.* The reported enhancement of the dielectric constant is normally associated with the increase of impurity concentration n in doped semiconductors or metallic component p in conductor-dielectric mixtures. When n (or p) reaches a threshold n_c (p_c), the dielectric constant of these materials usually exhibits a divergence.

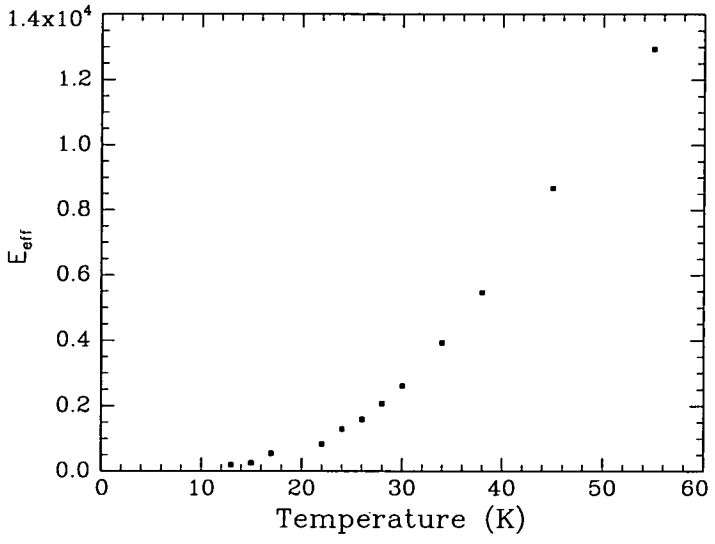

Fig. 10. Change of ε_{eff} with temperature.

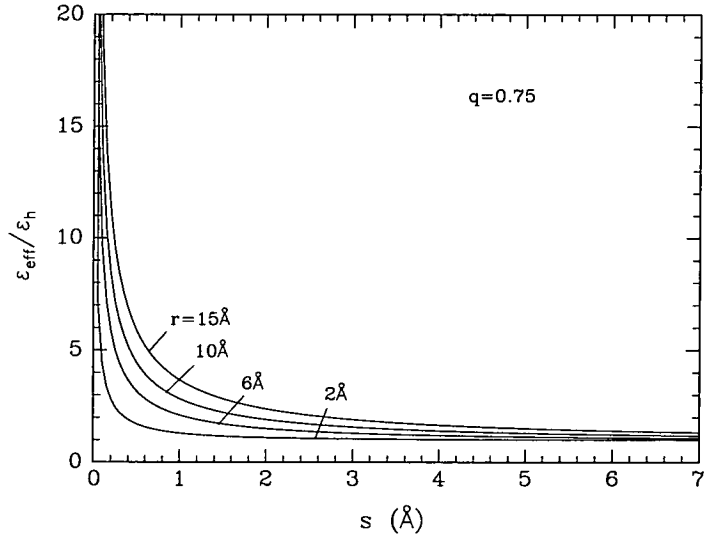

Fig. 11. Change of $\varepsilon_{eff}/\varepsilon_h$ with s for the radius range of 2~6$\dot{A}$.

In the present case of a temperature-induced MNM transition, it is possible that the temperature may affect the distribution of metallic particles inside the conducting filament, or more specifically, inside the remaining a-Si:H area, so that ε_{eff} shows an anomalous change. In the following we apply percolation theory to describe ε_{eff}. In this way, we can correlate the change in ε_{eff} with the microstructure of the filament.

According to percolation theory, the effective static dielectric constant can be expressed by the following formula (A.P.Vinogradov *et al.*, 1984; Herman *et al.*, 1984):

$$\varepsilon_{eff} \sim \varepsilon_h \left| \frac{p - p_c}{p_c} \right|^{-q} \tag{7}$$

where q is the critical exponent, $q \sim 0.75$ and ~ 1.3 for three-dimensional and two-dimensional heterogenous conductor-dielectric binary composites respectively. ε_h is the dielectric constant of the host material, and p and p_c are the volume fraction of the particles and the threshold respectively. Assuming that the remaining a-Si:H layer (see Fig.8(c)) has a cylindrical shape with diameter d and thickness D, and the embedded particles are spheres with the radius r, then ε_{eff} can be related to the spacing s between particles and their radius r:

$$\varepsilon_{eff} \sim \varepsilon_h \left| \frac{kr^3/(s+r)^3 - p_c}{p_c} \right|^{-q} \tag{8}$$

where k is a constant. The geometric factor, i.e. d^2/D, can be calculated using the standard capacitance equation:

$$C = \frac{\varepsilon_{eff} \varepsilon_0 A}{D} \tag{9}$$

where $A = \pi d^2/4$ is the area of a-Si:H layer. The ratio of d^2/D is nearly a constant as the temperature changes from $13K$ to $55K$. If D reduces to $\sim 10\dot{A}$ after the forming process, d would be about $5\mu m$ equal to half of the original pore diameter ($10\mu m$). The remaining a-Si:H layer therefore can be treated as a two-dimensional composite film (since $d \gg D$), and the critical exponent q thus is chosen as ~ 1.3.

The dimension of the embedded particles inside the a-Si:H layer can be estimated from the activation energy. The electron transport in a-Si:H containing metallic particles could be assumed to be an activated tunnelling process. The activation energy ΔE is related to the particle radius r by (C.A.Neugebauer and M.B.Webb, 1962)

$$\Delta E = \frac{e^2}{\varepsilon_r \varepsilon_0 r} \tag{10}$$

Using experimental data of $\varepsilon_r = \varepsilon_{eff}$ (~ 1500) and $\Delta E = \Delta E_1$ ($1.8 \sim 6.2meV$), the radius of the particles is in the range of $1.6 \sim 5.3\dot{A}$.

The critical volume filling factor is treated as an adjustable parameter. The change of $\varepsilon_{eff}/\varepsilon_h$ with s for different r is shown in Fig.11, where $p_c = \pi/6$. As expected, the effective dielectric constant increases with the decrease of the separation of particles, and diverges as s approaches zero. The relative change of the effective dielectric constant has almost same magnitude as that shown in the experiments, i.e. for the particles with radius of $2\dot{A}$, $\varepsilon_{eff}/\varepsilon_h$ increases from ~ 1.03 to 18.6 when s decreases from $\sim 5\dot{A}$ to $\sim 0.07\dot{A}$, compared to the increase of $\varepsilon_{eff}/\varepsilon_h$ from 1 to 16, found experimentally. Therefore, the enhancement of C can be explained in terms of a percolation-like critical behaviour of the dielectric constant, which diverges at the threshold p_c.

5. CONCLUSION

AC characteristics of a-Si:H memory devices show a metal-non-metal transition with the change of temperature and have been analysed using multi-component RC and RL equivalent circuits below and above the MNM transition region. The anomalous behaviour of the filament capacitance is explained in terms of a percolation-like critical behaviour of the dielectric constant ε_{eff}, which diverges at the threshold p_c. The analysis shows that the structure of formed $Cr/p^+a-Si:H/V$ devices could be modelled as an extremely thin heterogeneous medium composed of metallic particles and insulator host (e.g.a-Si:H),

together with a metallic inclusion. These metallic particles originate from the diffusion of the top vanadium electrode during the forming process. The enhancement of the dielectric constant (capacitance) is due to the decrease of the separation (s) between these metallic particles. When $s \rightarrow 0$, the volume fraction of the metallic particles approaches its critical value, p_c, which is interpreted to be the point when the metallic spheres make contact. Thus the device undergoes a metallic transition.

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